ELECTRONOTES

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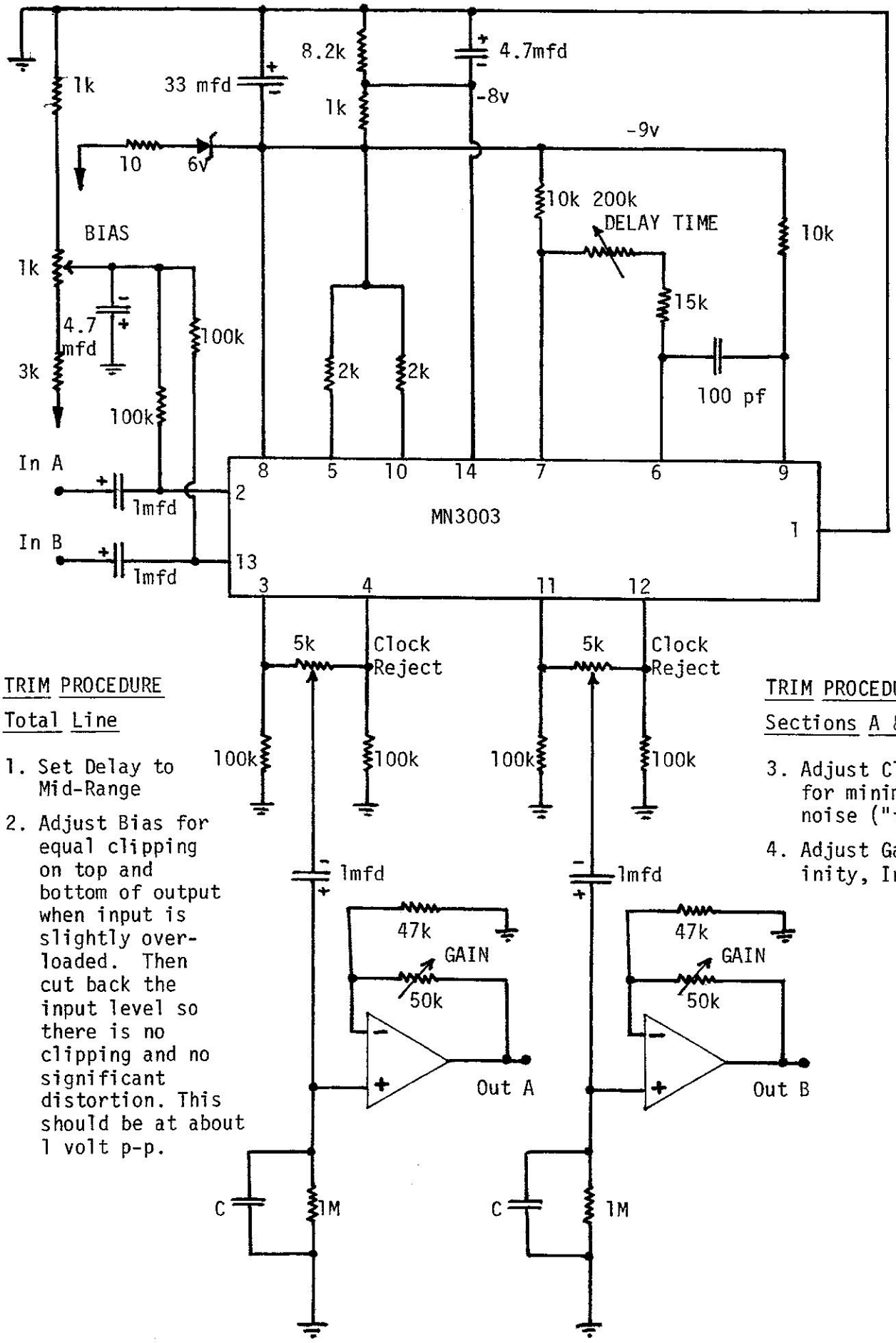
DELAY LINE SETUP WITH MN3003

We have in the past discussed delay line setups using bucket-brigade type analog delay lines. In AN-34 we showed a setup for the MN3001 and in AN-35, it was the SAD-1024, both of which are functionally equivalent, and are dual 512 stage delay lines. The MN3003, like the MN3001 is a bucket brigade type made by Matsushita. However, it is simpler in several ways. First, it has only 128 stages total in a dual 64 stage format. Secondly, the clock drivers are on the chip, and thirdly, it is also possible to use internal clocking with on-chip components. In line with this idea of simplicity, our setup is simplified over that of the earlier delay lines. We have taken out the voltage-controlled clock, the voltage-controlled filtering, and the DC coupling. This leaves us with little more to do than supply the proper supply voltages, set up the internal clock, and boost the output gain slightly.

The circuit of the setup is shown in the figure on the back of this note. The delay line chip runs on -9 volts, and also needs two other bias voltages, -8 and an input DC bias voltage of about -4.2. We start with a basic standard ±15 volt supply. The -9 volt supply is obtained from the -15 by using the 6v Zener diode and the 33mfd capacitor. The 10 ohm resistor limits the current on power-up, but otherwise has no real effect. The voltage divider of 1k to 8.2k serves to divide down the -9 to get -8 volts, and this is filtered by the 4.7mfd capacitor attached to the voltage divider node and pin 14 of the MN3003. The DC Bias viltage is variable from -3 to -6, is filtered by a 4.7mfd capacitor, and is fed to the input pins (2 and 13) of the MN3003 through 100k resistors. The actual AC signal is coupled in through 1 mfd capacitors. The delay time is variable from about 0.3 ms to 3ms by adjusting the 200k "Delay time" pot. The timing capacitor is the 100 pf capacitor between pins 6 and 9 of the MN3003. The two outputs each have two terminals each, and a trimmer selects a mix between these two and is adjusted for maximum clock rejection. The signals are then AC coupled out and amplified by the op-amps. These op-amps have a gain of from 1.0 to 2.0, with a gain of about 1.5 being the usual setting of the trimmer.

As with any discrete time system, it is necessary to limit the bandwidth of the input signal. Each section of the 3003 has 64 stages, which for a bucket-brigade amounts to 32 samples, so the clocking rate on the line is 32/D where D is the delay. For a 1 ms delay, the clock rate would be 32 kHz, and the bandwidth must be limited to half this or 16 kHz. While 16 kHz is a reasonable bandwidth for audio, we must realize that practical input guard filters have a finite roll-off rate, so for the 32 kHz clock rate, a bandwidth of less than 16 kHz must be used in practice. Thus, an audio signal with a 16 kHz bandwidth can be delayed only for values of time of less than 1 ms. For the best input guard protection, it is desirable to make sure the roll-off is sufficient to bury any frequencies that exceed the bandwidth of the line in the background noise. For practical purposes, 40db should do, which is achieved with a fourth-order filter and a little less than 2 octaves roll-off room.

It is also necessary to have an output smoothening filter of some sort. Here we achieve output smoothening with the capacitor C. Note that the output impedance of the delay line (with associated resistors), the 1 mfd output capacitors, the 1 meg resistors on the (+) input of the op-amps, and the capacitors "C" form a series high-pass and low-pass combination. The high-pass serves to AC couple while the low-pass serves to smoothen. C should be in the range of 100 pf to 500 pf for most applications. It is best to test the filter experimentally. This can be done by setting the delay line to minimum delay, and then testing the delay line, input to the output of the op-amps.



TRIM PROCEDURE

Total Line

1. Set Delay to Mid-Range
2. Adjust Bias for equal clipping on top and bottom of output when input is slightly over-loaded. Then cut back the input level so there is no clipping and no significant distortion. This should be at about 1 volt p-p.

TRIM PROCEDURE

Sections A & B

3. Adjust Clock Reject for minimum clock noise ("fuzz")
4. Adjust Gain for inity, In to Out