lower first three harmonics (for medium levels of loudness), and then tended to have a bump of harmonics somewhere up around, an extremely subjective, range of their 7th to 12th harmonics. Note also that the Echo-Harp of Fig. 7 had two reeds per note that were off in frequency by a couple of Hertz. This arrangement gave the instrument a mellow choral effect and also provided a slow pleasant beating to its music.

III. BENDING OF NOTES . . . JUST FOR FUN:

The last section of this paper deals very briefly with bending a note of a harmonica. This is what it is called when, by redirecting the flow or air and its velocity by use of the tougue, mouth, and throat, one is able to make a note go temporarily flat to a varying degree. Fig. 9 and the following small figures demonstrate how a harmonica can be "bent" flat so as to produce a "blues" type of sound or crying effect.

Also included, just for fun, is a plot of the harmonicist's next best friend, the Jaw-Harp (or Jew's-Harp). It's familiar "twangy" sound has captivated people for thousands of years and it too is capable of altering its spectral content in the hands, or should we say mouth, of any "skilled" well-rounded musician.

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BUILD A PRECISION CONTROLLER CLOCK:

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Described herein is a circuit for a precision controller clock suitable for the most demanding low frequency applications. For realtime use, the controller clock is handy for firing sequencers, sample-and-holds and automatic drum units and in the recording studio it is equally useful for creating precise, repeatable sync tracks. In short, the controller clock may be used whenever a source of precisely timed triggers is needed. The features of this circuit are summarized:

- [] 1 volt per octave response
- [] variety of period control options
- [] periods from 2 minutes to 1 millisecond; seventeen octaves
- [] precision gating for start and stop of output
- [] manual or trigger gating modes
- [] standard gate, trigger and ramp outputs
- [] extremely precise 50% duty cycle
- [] simple design employing the CEM3340 VCO chip

The value of most of these features should be obvious, but several deserve a little more description. Precision gating implies that the clock should begin and end oscillation at well defined states only. For example, a start trigger should start the clock oscillating, with the very first cycle going high and maintaining standard pulse width. A stop trigger should gate the clock off, but only when the output has first gone low (end of cycle). A "memory" remembers that a stop is desired, and the next time the output goes low, the clock is gated off. So, precision gating means that the clock starts by instantaneously initiating a normal cycle and stops only when the output next goes low.

The start and stop signals may be delivered to the unit manually or by means of a trigger. Thus, clock operation can be controlled by either depressing pushbuttons or having a standard synthesizer keyboard send electrical triggers which initiate the gating action.

Before examining the circuit, a few words should be said concerning the accuracy and reliability of the unit. Rather than simply taking the pulse output of the CEM3340 VCO chip (which forms the heart of the controller clock), the signal is first sent to a seven stage binary divider, with switch selectable taps. By dividing the signal down, four major benefits are reaped. First, most VCO's have the best accuracy when they are operating in the middle of their oscillation range. Exponential conversion errors, offsets and leakage currents can be a problem when the VCO is operated toward its lower limit; be forcing the oscillator to operate at a higher frequency and then dividing downward, these problems are avoided. Secondly, it has been shown that binary division acts as a "vibrato killer". [1] Thus, any undesired FM deviations and irregularities in the original VCO signal are averaged out before hitting the final clock output. Next, binary dividers have edge sensitive clock inputs. This implies that the output signal will have a precise 50% duty cycle regardless of any fluctuations of the input duty cycle. Finally, by making the divisor of the binary divider switch selectable, an even greater frequency range can be obtained. In summary, then, by using the simple notion of binary division, a very precise output in both frequency stability and duty cycle is obtained over a broad range of frequencies.

Fig. 1 shows the complete schematic for the precision controller clock: refer to it now. IC1 is the CEM3340 VCO chip which forms the heart of the unit. Pin 15 of this chip is a summing node and may accept a variety of control voltages. A 1V/octave control from a keyboard, say, may be applied via jack J1. In the context of period generation (as opposed to frequency generation), an increase of one volt at this input causes a decrease of period by a factor of two. A control voltage also may be applied to the controller clock via jack J2, and in this case, the signal can be atteunated by R38 as desired. Typically, envelope of LFO control signals would be applied to this input and R38 allows these to be "tamed". Finally, R36 and R37 form the fine and course rate controls. These two controls are strung across the entire bipolar supply and this facilitates compensating for offsets in control signals applied to either J1 or J2.

J4 is the start signal input. A logical signal of about five volts or more (in either gate or trigger form) applied to this input will start the controller clock oscillating. Oscillation begins immediately with a first cycle of normal pulse width. C3 and R32 differentiate the input signal while A2, R23 and R13 shape it up into a rectangular pulse about 1 millisecond wide. D6 blocks negative excursions of comparator A2, thus making the pulse polarity compatible with the remaining CMOS circuitry.

S2 is the manual start pushbutton; since its output is applied to an R-S flip-flop (see below), no switch debounce is necessary. The output of S2 is normally held low by R26. Depressing the switch developes a voltage of +15 volts across this resistor, and D7 conducts the result to later circuitry. Note that in this context, D6 and D7 (which apply voltage across R27) form a simple OR gate. This is an instance of "Mickey Mouse" logic, which despite the disparaging name is a valid logic technique. [2]

The start signal (from either J4 or S2), resets both of the R-S flip-flops via pins 4 and 10. In the former case, the $\overline{Q}$ output (Q-bar) at pin 2 goes high and in the latter case, the Q output at pin 13 goes low. When the Q output goes low, IC1 is enabled via R20 and Zener diode D3 (more about this shortly). Simultaneously, pin 2 of IC2 is brought low, thus enabling the seven stage counter. The VCO starts oscillating and the counter starts counting. Notice that the pulse output of the CEM3340 is taken off pin 4. Voltage divider R16 and R30 set the pulse width of the CEM3340 to about 50% and C4 prevents bounce and chatter of the pulse wave at low frequencies. [3] The output of the counter (which is the complement of the desired waveform) is tapped via switch S3 and sent to gate N3 where it is NORed with the Q output of IC3. Recall that this signal is currently in the low state so that N3 inverts the counter output, thus restoring the desired polarity.

The stop circuitry (A1 and associated components) is identical to the start circuitry. Again, two diodes, D4 and D5, OR the signals, and the result is sent to the SET input of the R-S flip-flop at pin 6. A stop signal causes pin 2, the $\overline{Q}$ output, to go low. This condition is echoed to NOR gate N2, whose output controls the second R-S flip-flop. Notice that the output of N2 will go high only when the counter output

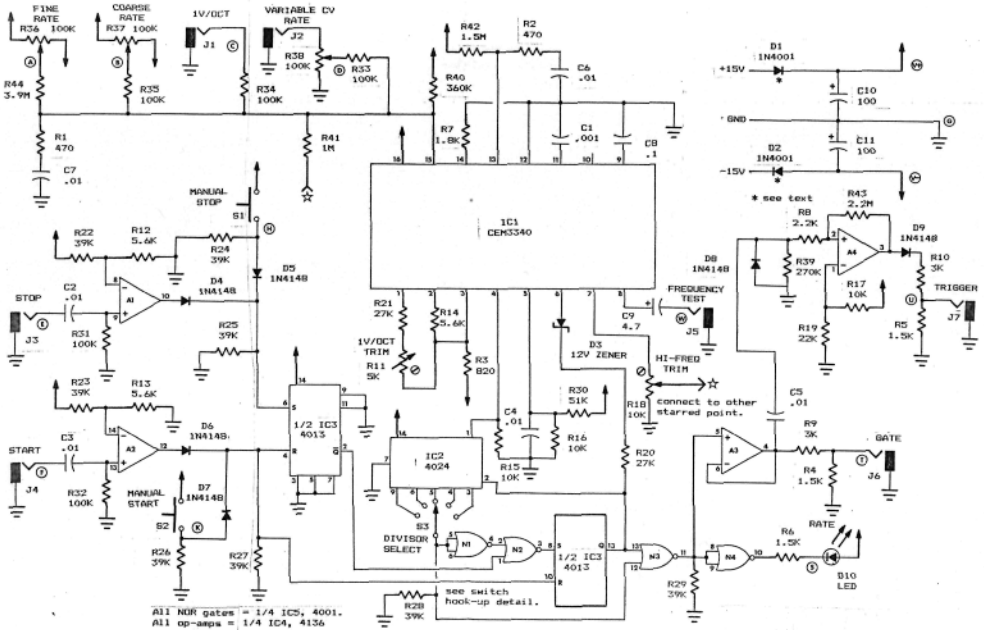
FINE RATE R36 100K
COARSE RATE R37 100K
1V/OCT
J1
VARIABLE CV RATE
J2
R38 100K
R33 100K
R34 100K
R35 100K
R44 3.9M
R1 470
C7 .01
R41 1M
R42 1.5M
R2 470
R40 360K
R7 1.8K
C6 .01
C1 .001
C8 .1
1C1 CEM3340
D1 1N4001
+15V
C10 100
GND
C11 100
D2 1N4001
-15V
* see text
R43 2.2M
R8 2.2K
D9 1N4148
R10 3K
TRIGGER
J7
R39 270K
R17 10K
R19 22K
R5 1.5K
D8 1N4148
MANUAL STOP
S1
R22 39K
R12 5.6K
R24 39K
D5 1N4148
STOP
J3
C2 .01
A1
D4 1N4148
R31 100K
R25 39K
R21 27K
R14 5.6K
1V/OCT TRIM R11 5K
R3 820
C9 4.7
FREQUENCY TEST
J5
D3 12V ZENER
HI-FREQ TRIM R18 10K
connect to other starred point.
C5 .01
R30 51K
R16 10K
R20 27K
R15 10K
C4 .01
R23 39K
R13 5.6K
D6 1N4148
START
J4
C3 .01
A3
R32 100K
MANUAL START
S2
D7 1N4148
1/2 IC3 4013
IC2 4024
S3 DIVISOR SELECT
N1
N2
N3
N4
1/2 IC3 4013
R9 3K
GATE
J6
R4 1.5K
RATE
R6 1.5K
B10 LED
R26 39K
R27 39K
R28 39K
see switch hook-up detail.
R29 39K
All NOR gates = 1/4 IC5, 4001.
All op-amps = 1/4 IC4, 4136
PRECISION CONTROLLER CLOCK
DESIGNER: Thomas Henry
All resistors in ohms.
All capacitors in mfd.
(circle) keys schematic to printed circuit board.

FIG. 1

ENFE (13)

has gone low. The net effect is that the clock will not be gated off until the output attains its next low state. This is part of the precision gating requirement mentioned above. It is interesting to note that IC3 is really acting like a "memory" here; it acknowledges that a stop signal has been sent, remembering it until the time is right to shut off the oscillator.

When N2 is high, the flip-flop is set thus sending the Q output at pin 13 high. This does two things. First, IC2 is gated off via pin 2. Likewise, IC1 is shut off via R20 and Zener diode D3. This scheme for gating the CEM3340 first appeared in the now defunct (and greatly missed) house journal for Curtis Electromusic Specialties, Synthisource. [4] The reader is referred to this reference for further information on this important topic.

The Q output is NORed with the output of the seven stage counter, IC2. This insures that the final clock output is held in a low state when the oscillator is off and likewise guarantees that the output starts by going high immediately upon detection of a start signal. D10 monitors the output. When the clock is off, so is the LED: when the clock is on, the LED flashes at the selected rate.

A3 buffers the CMOS signal for real world interfacing. The output is chopped down to standard 0V to +5 volt size by voltage divider R9 and R4, which also provides a standard 1K output impedance. This forms the gate output, which will have a 50% duty cycle.

C5 couples the signal to A4 and associated circuitry which creates a nominal 1 millisecond output trigger. D8 dumps the negative swing of differentiator C5, while R39 provides the damping. A4 forms a Schmidt trigger, which gives a sharp output signal. D9 restricts the polarity of the output, while voltage divider resistors R10 and R5 bring the signal down to a standard 0V to +5V swing.

J5 provides a "frequency test" output which is actually nothing more that a 10V pp ramp wave. This output, which runs at the VCO's normal frequency, is provided for several purposes. First, it's a convenient output to monitor when tweaking the scale trimmer for a precise 1V/octave response. Secondly, when using the excellent method of frequency-to-period conversion for playing complex rhythmic patterns by sequencer, the "frequency test" output may be used to set the desired interval. [5] This greatly speeds up the adjustment of sequencers and makes the technique that much more automated. Lastly, the controller clock may be used just like any VCO, and in this context, the ramp output with its even order harmonics is a pleasant sound source.

Finally, trimmer R11 can be used to adjust the scale for a precise 1V/octave response. Trimmer R18 allows for compensating the high frequency response droop (caused by exponential conversion errors and to a lesser extent, to reset lag time).

Building the controller clock is straightforward, but some attention must be paid to circuit layout. This is especially true around pins 15, 13 and 11 of the CEM3340 (which are the exponential input, the reference current and the timing capacitor pins, respectively). Neatness really counts here! The best way to go is with a printed circuit board which eliminates many of the problems of "rat's nest" wiring. To simplify the task of generating a circuit board for this project, Fig. 2 shows the lifesize artwork for a tested design. This copyrighted circuit may be fabricated by individuals for their own use, but commercial users should contact the author at the above address for licensing details.

Fig. 3 shows a parts placement guide for the circuit baord. When loading the board, be sure to observe the polarity of all diodes and electrolytic capacitors, and be certain to orient the IC's correctly. A number of jumpers are needed and these are denoted on the parts placement guide by the letter "J". You may use resistor clippings or bare bus wire for these. Notice that the circled letters in the schematic of Fig. 1 call out the various input and output pads to the circuit board. Thus the schematic may be used as the main wiring guide for the circuit. Fig. 4 shows a detail of switch S3 and makes it clear how to proprely wire up this

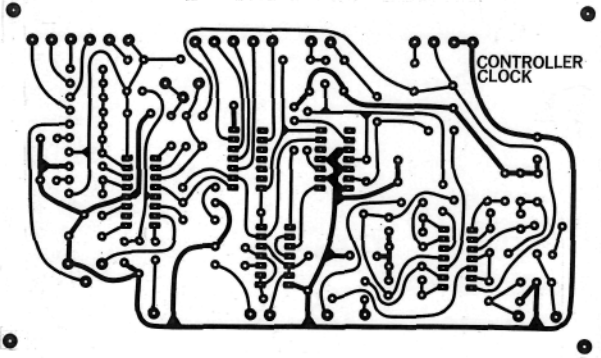

Fig. 2 Printed Circuit Board Layout

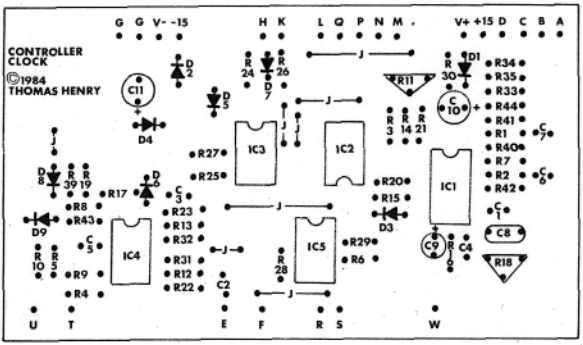

Fig. 3 Part Placement Guide

five position rotary switch. Power is supplied to the board at the points labeled +15, G, and -15. Points V+ and V- may be used to run the supply limits to the front panel controls (like the tuning pots, the pushbuttons and the LED). The pads labeled G, of course, are the ground connections.

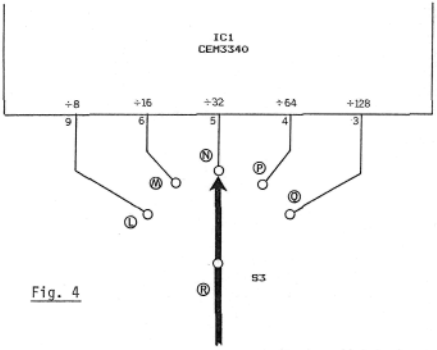

Fig. 4

Detail for switch hook-up.

(circle) keys schematic to printed circuit board.

Rectifiers D1 and D2 and capacitors C10 and C11 provide a measure of decoupling for the controller clock from other circuits running off the same power supply. However, in the original prototype it was found that D1 and D2 raised the impedance of the power supply, as seen by the circuit, sufficiently to inject some undesired FM effects. It was found that the LED flashing caused enough of a differential current flow to actually impose a vibrato on the VCO (probably through the tuning controls or R40). This vibrato effect was very slight, on the order of 10 cents or less at the ramp wave output, and had no perceptible effect on the gate or trigger outputs (for reasons mentioned earlier concerning the benefits of binary division). Nonetheless, its effect on the ramp wave was annoying enough to suggest replacing diodes D1 and D2 with jumper wires. This, in fact, cured the problem in the prototype, so if frequency deviation problems occur, try replacing the rectifiers with jumpers. As mentioned above, D1 and D2 were originally added to aid in the decoupling of this circuit (they act like low valued resistors and form an RC network with C10 and C11). In retrospect however, it should have been clear that the disadvantages of raising the effective output impedance of the power supply far outweigh the benefits of improved decoupling. In general, VCO's need tightly regulated power supplies and nothing should come between the supply and the VCO!

Fig. 5 gives the complete parts list for the circuit. After finishing construction, using Figures 1 and 5 as a guide, apply power to the unit. Confirm that the start and stop functions work correctly and then test the various outputs for proper waveshape and amplitudes. If everything checks out, the controller clock may be tweaked. First, turn trimmer R18 to the ground position, thus injecting no correction voltage into the circuit. Now, while monitoring the ramp wave output, adjust R11 for a 1V/octave response in the range of 500 Hz. A standard synthesizer keyboard may be used to supply the control voltages for this step. Next adjust the high frequency trimmer, R18, for the same response in the region of about 5 KHz. This completes the alignment of the controller clock but after a burn-in time of several hours, the trimmers should be realigned for maximum accuracy.

As mentioned at the start of this article, the uses for a controller clock are

Fig. 5 CONTROLLER CLOCK: PARTS LIST

RESISTORS

R1, R2	470 ohms
R3	820 ohms
R4-R6	1.5K
R7	1.8K
R8	2.2K
R9 - R10	3K
R11	5K trimmer
R12 - R14	5.6K
R15 - R17	10K
R18	10K trimmer
R19	22K
R20, R21	27K
R22 - R29	39K
R30	51K
R31 - R35	100K
R36 - R38	100K linear pot
R39	270K
R40	360K
R41	1M
R42	1.5M
R43	2.2M
R44	3.9M

CAPACITORS

C1	.001 mfd poly
C2 - C7	.01 mfd mylar
C8	.1 disk
C9	4.7 mfd electrolytic
C10 - C11	100 mfd electrolytic

SEMICONDUCTORS

D1, D2	1N4001 (*)
D3	12V Zener
D4 - D9	1N4148
D10	LED
IC1	CEM3340 VCO chip
IC2	4024 ripple counter
IC3	4013 dual flip-flop
IC4	4136 quad op-amp
IC5	4001 quad NOR gate

(*) see text

MISCELLANEOUS

J1 - J7	1/4" phone jacks
S1, S2	SPDT pushbutton switch
S3	SP5T rotary swithc

LED holder, wire, solder, knobs, front panel, hardware, etc.

myriad. But its value is really apparent when the clock is used to fire sequencers. For example, a two bank sequencer may devote the second bank for setting the duration of each of the notes, using the method described elsewhere by Duesenberry. [5] The period-to-frequency conversion method is applicable here since the controller clock has a standard 1V/octave response. And, or course, the gating feature will be handy for percussion and sync effects in the recording studio. All and all, while the controller clock may not be the most glamorous of synthesizer modules, there is no doubt that it makes possible a number of effects which would be difficult or even impossible to accomplish any other way.

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[1] Bernie Hutchins, "The Digital Divider as a 'Vibrato Killer' ", Electronotes, Vol. 12, No. 119, Nov. 1980, pg 2

[2] Don Lancaster, CMOS Cookbook, (indianapolis: Howard W. Sams and Co. 1977) pp 186-189

[3] Doug Curtis, "Comments on 'Two Hints on Using the CEM3340 VCO IC' ", Electronotes, Vol. 13, No. 122, Feb 1981, pg 2

[4] Anonymous (suggested by an idea of John McColm), "Reader's Circuit Corner", Synthisource, Vol. 1, No. 2, Spring/Summer 1981, pp 13-15

[5] John Duesenberry, "Rhythmic Control of Analog Sequencers", Polyphony, Sept/Oct. 1978, pp 26-29