ELECTRONOTES 194

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GROUP ANNOUNCEMENTS

CONTENTS OF EN#194

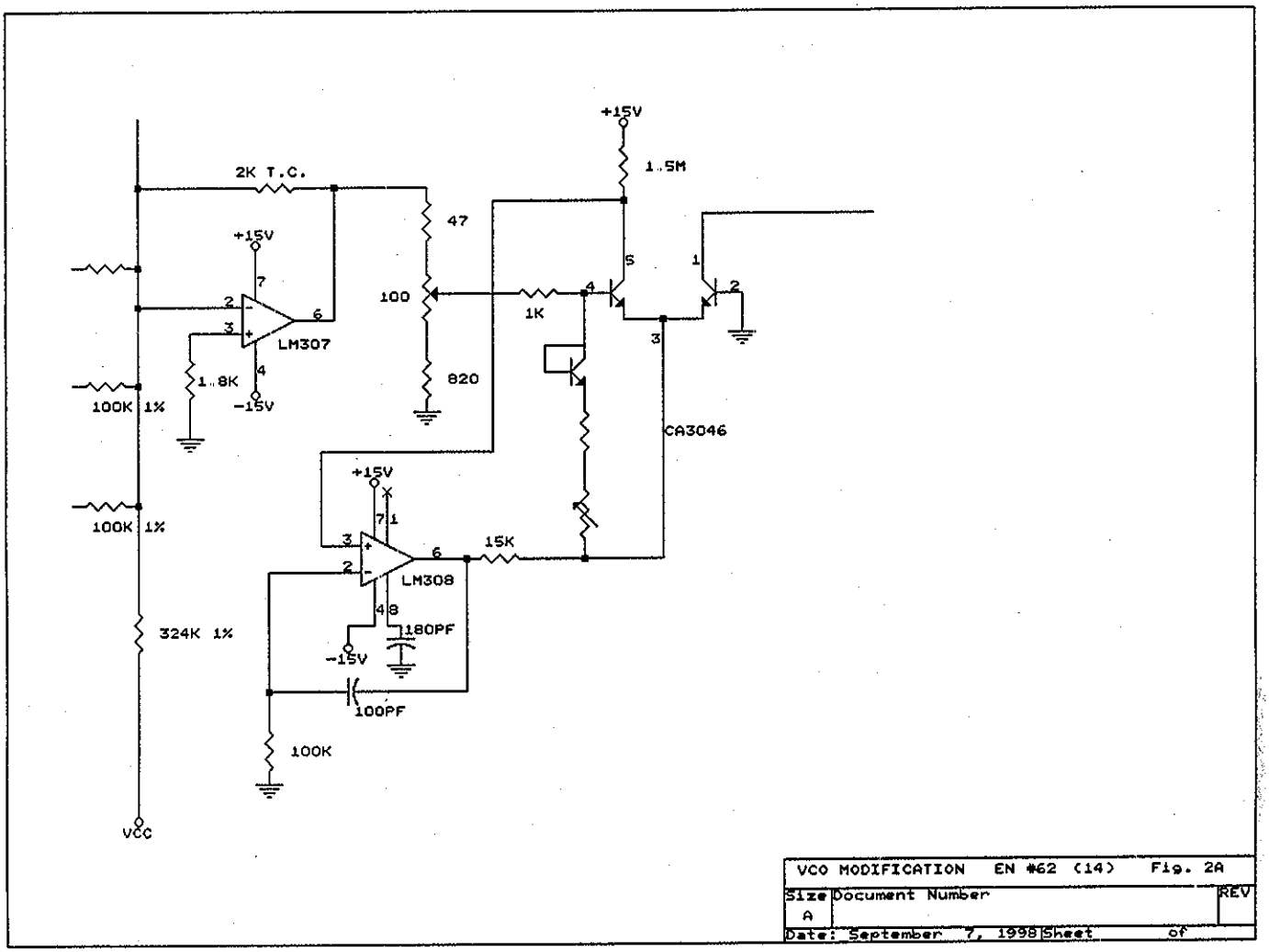
This issue covers Chapters 5 and 6 of Analog Signal Processing. Both these chapters expand on the repertoire of design configurations, to include at least two active ladder methods, through the use of "gyrators" or "supercapacitors" (Chapter 5) and through the use of integrators in a flow-graph simulation (Chapter 6). Chapter 7, a very long chapter, deals with the non-ideal aspects of the various configurations considered.

This issue begins with a "blast from the past" item, which is a modification to a classic and popular VCO circuit which first appeared in EN#62 (Feb. 1976) and reappeared in its basic form in a number of subsequent designs, including the well-received ENS76 Option 1 VCO. Here Terry shows us a different way of doing the high frequency tracking.

MODIFICATIONS TO A VCO DESIGN FROM 1976

Along with Dave Rossum, Ian Fritz, and many others who contributed circuits for our readers, Terry Mikulic was well represented and often gave us extremely good designs. Often these arrived at times that were perfect in terms of assembling our complete ensemble of modules. Terry's VCF design provided the basic ideas of most of our CA3080-based state-variable designs. The VCO in EN#62 (Feb. 1976) became a prototype for all our later sawtooth-based VCO's, as I recall. It was a great pleasure to

have him call a few months back, and receiving the circuit diagram with VCO modifications was certainly remindful of the good old days.



CHAPTER 5

ADDITIONAL CONFIGURATIONS

5-1 ADDITIONAL LOW-PASS CONFIGURATIONS:

We are familiar with the Sallen-Key low-pass structure which we have used in many of our examples. Here we will look at a few more low-pass options. Again, we use low-pass as an example, but the general ideas can be extended for other types of filter.

The Sallen-Key low-pass is also known as the Positive Gain VCVS (Voltage-Controlled Voltage Source), and the amplifier with gain of K is something we easily recall about Sallen-Key. As we saw, when we made the component values equal, we required a K greater than +1 for complex poles. Since the case of K=1 (a "buffer") is an easy op-amp circuit, and because other types of buffers are easily achieved (such as FET source followers, which can have superior high-frequency performance), we want to see what can be done with Sallen-Key with K=1 and allowing the component values to spread.

Fig. 5-1 shows the Sallen-Key structure with K=1, and where we are now specifically suggesting that C_1 need not equal C_2, and R_1 need not equal R_2. For this case, the transfer function can be obtained and put in the form:

$$T(s) = \frac{1/R_1R_2C_1C_2}{s^2 + \frac{1}{\sqrt{R_1R_2C_1C_2}}\frac{(R_1+R_2)\sqrt{C_2}}{\sqrt{C_1R_1R_2}}s + \frac{1}{R_1R_2C_1C_2}} \qquad (5\text{-}1)$$

from which we can easily write down the design equations:

$$f_{sd} = 1/2\pi\sqrt{R_1R_2C_1C_2} \qquad (5\text{-}2)$$

$$D = \left[\sqrt{\frac{R1}{R_2}} + \sqrt{\frac{R2}{R1}}\right]\sqrt{\frac{C2}{C1}} \qquad (5\text{-}3)$$

We note that in the case $R1=R2$ and $C1=C_2$, equation (5-3) gives D=2, which agrees with the K=1 limit of our earlier studies of Sallen-Key. Our next thought would be to try to hold $C_1=C_2$, and try to achieve values of D that are less than 2 by varying R1 and R_2. However, in such a case $D = [(R1/R_2) + (R2/R1)]$ which has a minimum value of 2 when $R_2=R1$. Accordingly, we are not going to be successful unless we concede that there has to be a spread between C_1 and C_2. If we then take $R1=R_2$, equation (5-3) becomes:

$$D = 2\sqrt{C_2/C_1} \qquad (5\text{-}4)$$

From this relatively simple result, it is fairly easy to design low-pass sections, and have an overall dc gain of 1. Note that a simple 2nd-order Butterworth is achieved with $C_1=2C_2$. It is usually not difficult to obtain this 2:1 ratio. If necessary, three equal valued capacitors can be used, with a series or parallel combination of two of them being used to obtain the 2:1 ratio needed.

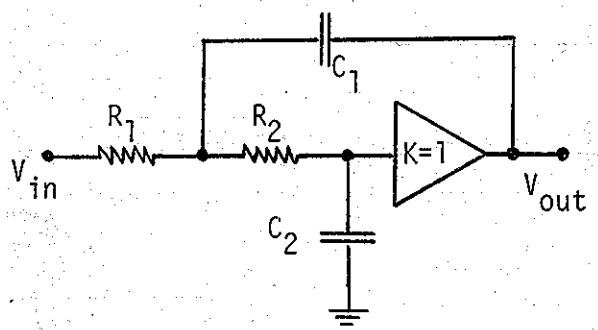


Fig. 5-1

Unity-Gain VCVS or Sallen-Key will require $C_2 \neq C_1$ for useful values of damping.

We are familiar with the Multiple-Feedback Infinite-Gain (MFIG) bandpass. MFIG configurations are also possible for low-pass and for high-pass, and in fact for all-pass and notch (see Section 5-2). The MFIG low-pass is seen in Fig. 5-2. Its transfer function can be obtained and put in the form:

$$T(s) = \frac{-(R_3/R_1)(1/R_1R_3C_1C_2)}{s^2 + \frac{1}{\sqrt{R_2R_3C_1C_2}}\sqrt{\frac{C_2}{C_1}}\left[\sqrt{\frac{R_2}{R_3}}+\sqrt{\frac{R_3}{R_2}}+\sqrt{\frac{R_2R_3}{R_1}}\right]s + \frac{1}{R_2R_3C_1C_2}} \qquad (5\text{-}5)$$

from which the design equations are easily obtained as:

$$f_{sd} = 1/2\pi\sqrt{R_2R_3C_1C_2} \qquad (5\text{-}6)$$

$$D = \sqrt{\frac{C_2}{C_1}}\left[\sqrt{\frac{R_2}{R_3}}+\sqrt{\frac{R_3}{R_2}}+\frac{\sqrt{R_2R_3}}{R_1}\right] \qquad (5\text{-}7)$$

There are a number of component selections that can be tried here (see problem at end of chapter). One of the results of this component selection study is similar to that of the unity gain VCVS just studied: we must have some spread in the capacitors. If we do the next simplest thing, that of setting the resistors all equal to R, and set the capacitors so that $C_2 = BC_1$, we find equations (5-6) and (5-7) becoming:

$$f_{sd} = 1/2\pi\sqrt{B}RC_1 \qquad (5\text{-}8)$$

$$D = 3\sqrt{B} \qquad (5\text{-}9)$$

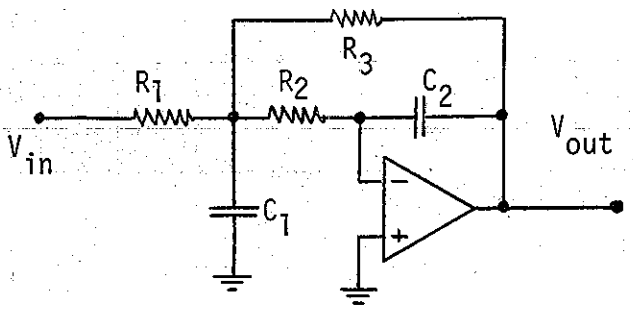


Fig. 5-2

MFIG Low-Pass

The third new low-pass configuration that we will look at is of the negative gain VCVS type, which we have not looked at before. The Sallen-Key used a finite gain that was positive, the MFIG used an infinite gain op-amp, and this one uses a finite gain that is negative. The negative gain VCVS structures are well regarded for their excellent passive sensitivity properties (Chapter 7). However, their active sensitivity is rather poor (again, Chapter 7) so they should only be used at lower frequencies (say under 1 kHz). None the less, the configuration should be something that the analog filter designer knows about, and one form of the low-pass negative gain VCVS is seen in Fig. 5-3a. Note that the negative gain VCVS here is shown as a triangular symbol marked -K. We specifically intend that K is positive here, so -K implies an inverting amplifier. With positive gain VCVS, we were able to take advantage of the very high input impedance of non-inverting stages. Here we have to recall that the inverting op-amp stage has a relatively low input impedance, equal to the resistor in the input leg. We are able to avoid this problem by making the input resistor a part of the circuit (Fig. 5-3b), the resistor R going to ground in Fig. 5-3a now becomes the resistor R going to virtual ground in Fig. 5-3b.

Analysis of either structure gives the correct transfer function, which is:

$$T(s) = \frac{-K/R^2C^2}{s^2 + 5s/RC + (5+K)/R^2C^2} \qquad (5\text{-}10)$$

The corresponding design equations are:

$$f_{sd} = \sqrt{5+K}/2\pi RC \qquad (5\text{-}11)$$

$$D = 5/\sqrt{5+K} \qquad (5\text{-}12)$$

From these results, we can begin to appreciate where some difficulty with this structure begins. For a second-order Butterworth, K is already 7.5, and for a 3db Chebyshev 2nd-order, K is 37, and so on. This compares with K values between 1 and 3 for Sallen-Key. If we are working with real devices which have a finite gain-bandwidth product, the more gain we ask for, the less bandwidth we have available. On the other hand, it is probably the large, negative feedback, that gives the configuration its excellent passive sensitivity.

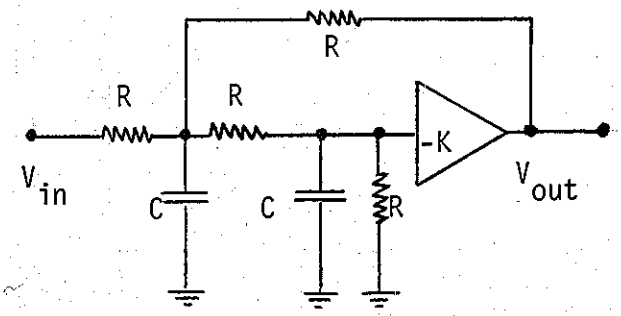


Fig. 5-3a Negative Gain VCVS Low-Pass (Note: K is a positive number here)

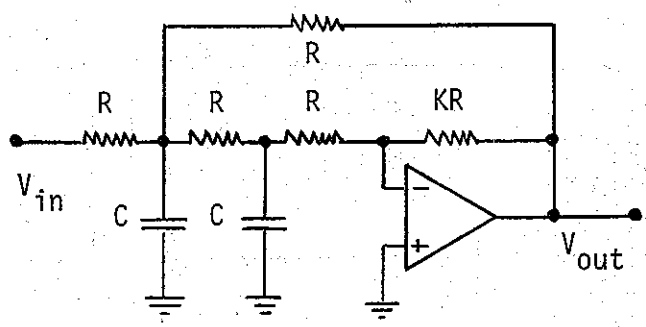


Fig. 5-3b Circuit of Fig. 5-3a showing realization of negative K.

It is worth mentioning that in both positive gain and negative gain VCVS configurations, the mathematical analysis is the same whether K is positive or negative. Negative values of K for Sallen-Key lead to overdamped filters. Negative values of K for negative-gain VCVS (meaning a positive gain amplifier) lead to an unstable filter for K more negative than -5, through an interesting path (see problems at end of chapter).

We will return to these three basic types, positive-gain VCVS, negative-gain VCVS, and MFIG in Chapter 7 when we discuss sensitivity. At that time, the state-variable structures of Chapter 6 will also be available for consideration.

5-2 CONFIGURATIONS EXTENDING THE M.F.I.G. BANDPASS:

A number of interesting extensions of the MFIG bandpass which we have studied can lead to higher Q bandpass filters, or to all-pass and notch filters. A general approach to this type of configuration can be achieved by first finding out what the transfer function is from the (+) input of the MFIG bandpass (which is normally grounded). To do this, we first consider a general network of passive components, as suggested in Fig. 5-4a. We assume that this network contains no sources, and no internal grounds. We also assume that we have access to three of the nodes of the network, and we will be concerned with the case where external voltage sources are applied to V_1 and V_2, and where the voltage V_3 is then measured open circuit (no current flows in or out of V_3. In this case, we can write, using superposition:

$$V_3 = T_1(s)V_1 + T_2(s)V_2 \qquad (5\text{-}13)$$

where $T_1(s)$ and $T_2(s)$ are transfer functions which we do not know. If we knew the details of the components inside the network, we could likely calculate these

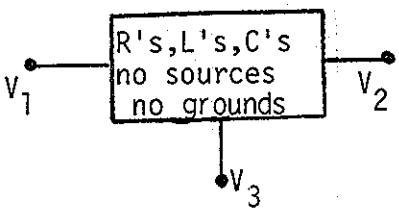


Fig. 5-4a

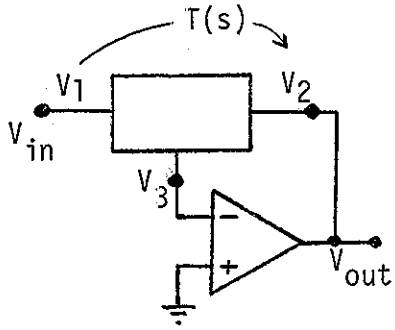


Fig. 5-4b

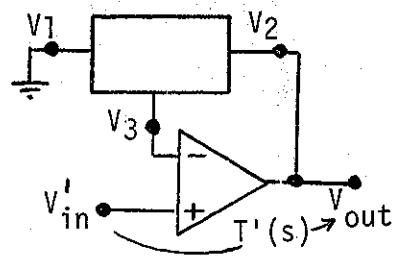


Fig. 5-4c

transfer functions, but these are not needed for our purposes here. We note from equation (5-13) that:

$$T_1(s) = [V_3/V_1]_{V_2=0} \tag{5-14}$$

and:

$$T_2(s) = [V_3/V_2]_{V_1=0} \tag{5-15}$$

The next point is to consider what happens if we connect V_1 and V_2 together and drive them with a single voltage source $V_1=V_2$. Because there are no sources or grounds inside the network, V_3 simply "floats" along at $V_1=V_2$. Another way to look at this is that since $V_1=V_2$, and since V_3 is open circuit, there are no potential differences possible inside the network, no currents flowing, and no voltage drops across components. Applying this to equation (5-13), we get:

$$1 = T_1(s) + T_2(s) \tag{5-16}$$

Now, while we do not know $T_1(s)$ or $T_2(s)$, because of the assumed nature of the network, we know that they sum to 1.

Next we assume that the network is employed as part of an op-amp circuit, as seen in Fig. 5-4b, and that the result is a transfer function T(s) as indicated. Here V_{out} takes on whatever value is necessary so that $V_3 = 0$ (the virtual ground idea). For this configuration, equation (5-13) becomes:

$$0 = V_{in}T_1(s) + V_{out}T_2(s) \tag{5-17}$$

or:

$$\frac{T_1(s)}{T_2(s)} = -\frac{V_{out}(s)}{V_{in}(s)} = -T(s) \tag{5-18}$$

which tells us that the ratio of the unknown $T_1(s)$ and $T_2(s)$ is related to the transfer function T(s) when the network is used as in Fig. 5-4b. [At this point, if we know T(s) we can solve for $T_1(s)$ and $T_2(s)$, but this is not what we are after at the moment.]

The final step which we need is to consider the use of the network in a different op-amp circuit, as in Fig. 5-4c. We do not know the transfer function T'(s) for this case, but equation (5-13) for this case gives:

$$V_{in}' = 0 \cdot T_1(s) + V_{out}T_2(s) \tag{5-19}$$

and since $T'(s) = V_{out}/V_{in}'$, we have:

$$T'(s) = 1/T_2(s) \tag{5-20}$$

Combining equations (5-16), (5-18), and (5-20) we obtain:

$$T'(s) = 1 - T(s) \tag{5-21}$$

The implication of equation (5-21) is that if we know T(s), we also know T'(s), the transfer function from the (+) input to the output. In a moment, we will apply this to the MFIG bandpass, but first we will look at a simple example.

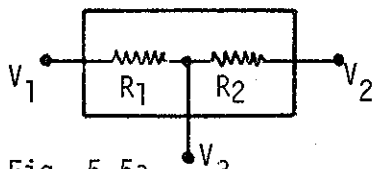


Fig. 5-5a

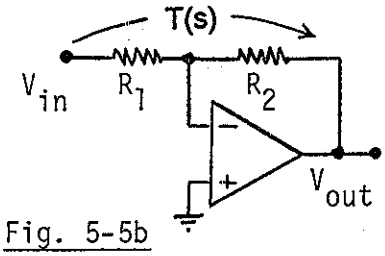


Fig. 5-5b

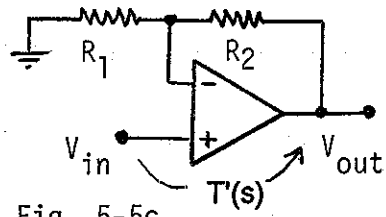


Fig. 5-5c

EXAMPLE 5-1 Verify equation (5-21) and equations leading to its development for the simple resistor network of Fig. 5-5a.

Since we know the network here, we can calculate $T_1(s)$ and $T_2(s)$ for easy use and reference. We have:

$$T_1(s) = R_2/(R_1+R_2) \tag{5-22}$$

$$T_2(s) = R_1/(R_1+R_2) \tag{5-23}$$

and we see that equation (5-16) is true for this case. Using the network as in Fig. 5-4b, we find our familiar inverting amplifier, Fig. 5-5b, for which we know:

$$T(s) = -R_2/R_1 \tag{5-24}$$

from which we see that equation (5-18) is true. Using the network as in Fig. 5-4c, we find our familiar non-inverting amplifier, (Fig. 5-5c), for which we know:

$$T'(s) = 1 + R_2/R_1 \tag{5-25}$$

which is in agreement with equation (5-20). Finally, equations (5-24) and (5-25) clearly obey equation (5-21) itself.

While equation (5-21) is of interest if we want to obtain T'(s) knowing T(s), it is more useful here in determining an output due to two inputs, one at the "normal" input, and the other at the (+) input. The total output is obtained using superposition. If the inputs are V_{in} and V_{in}' applied as in Fig. 5-6, we have:

$$V_{out} = V_{in}T(s) + V_{in}'[1 - T(s)] \tag{5-26}$$

We will be specifically interested in the case where V_{in} is not an independent second input, but rather some combination of V_{in} and V_{out}, or:

$$V_{in}' = KV_{in} + aV_{out} \tag{5-27}$$

where K and a are constants determined by certain network paths. In this case, equation (5-26) becomes:

$$V_{out} = V_{in}T(s) + (KV_{in} + aV_{out})[1 - T(s)] \tag{5-28}$$

We can now write a total transfer function as V_{out}/V_{in}, using equation (5-28) as:

$$T_t(s) = V_{out}/V_{in} = \frac{K + T(s)[1 - K]}{(1-a) + aT(s)} \tag{5-29}$$

Of course, when a and K are both zero, $T_t(s) = T(s)$.

Having now established the important equation (5-29) we will specifically be looking to apply this to T(s) of the MFIG bandpass, and for individual cases of

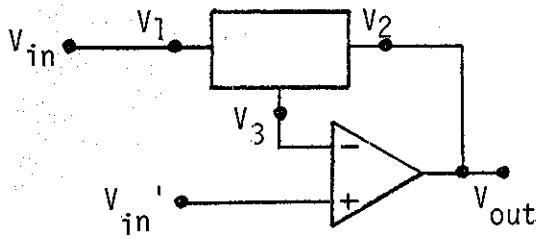


Fig. 5-6

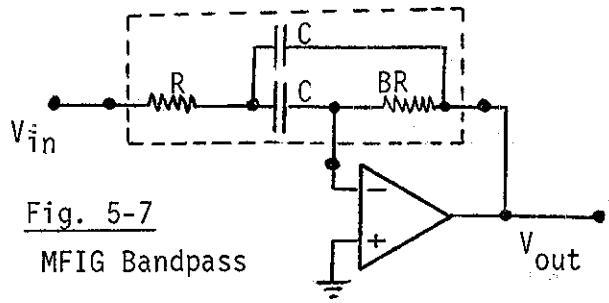


Fig. 5-7
MFIG Bandpass

feedback (K=0, a≠0) and of feedforward (K≠ 0, a=0). Fig. 5-7 shows the familiar MFIG bandpass, which has transfer function:

$$T_b(s) = \frac{-s/RC}{s^2 + \frac{2s}{BRC} + 1/BR^2C^2} \qquad (5\text{-}30)$$

where B is the resistor ratio shown. Note that the Q of this configuration is $\sqrt{B}/2$.

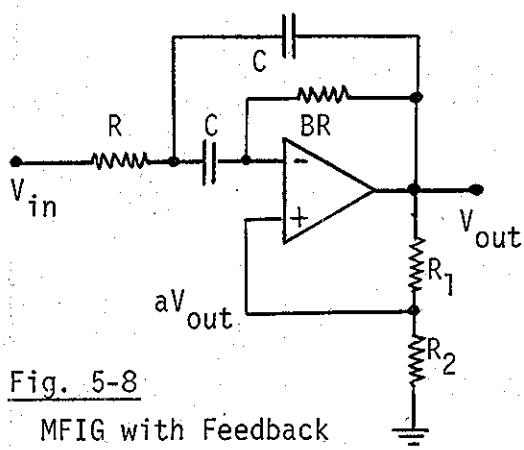


Fig. 5-8
MFIG with Feedback

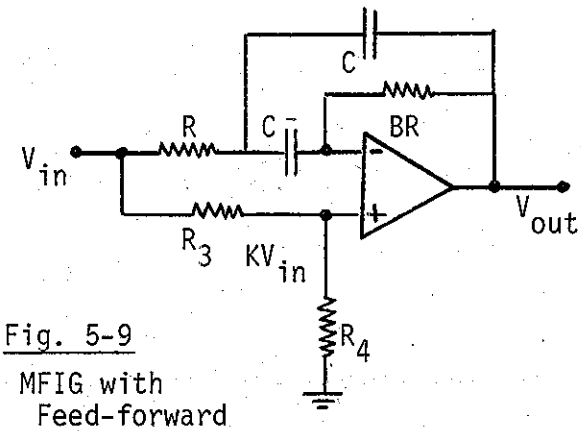


Fig. 5-9
MFIG with
Feed-forward

Fig. 5-8 shows the case where feedback is used. Here we have $a = R_2/(R_1+R_2)$. Applying equation (5-30) to equation (5-29), with K=0, we arrive at:

$$T_D(s) = \frac{T_b(s)}{(1-a) + aT_b(s)} = \frac{-s/(1-a)RC}{s^2 + \frac{s}{RC}\left[\frac{2}{B} - \frac{a}{1-a}\right] + 1/BR^2C^2} \qquad (5\text{-}31)$$

Here the D that is subscripted to T(s) indicates that this is the so-called "Deliyannis" bandpass structure, named after the person who first reported it. We note from equation (5-31) that the center frequency of the bandpass has not been changed by the feedback, although the Q and the peak gain have been changed. In fact, the Q is given by:

$$Q = \frac{\sqrt{B}\,(1-a)}{2(1-a) - aB} \qquad (5\text{-}32)$$

which in fact means that the Q is always increased here, relative to the normal MFIG bandpass. Note the usefulness of this in that we can first get the center frequency set, and have the Q come out somewhat lower than we want eventually. At this point, a bit of positive feedback will boost the Q to the desired value. In addition, somewhat higher values of Q can be obtained with this structure, without having to go to a very large value of B (spread of resistor values).

Actually, the Deliyannis bandpass is a specific example of a more general technique by which the Q of a bandpass filter can be adjusted. We can look at this

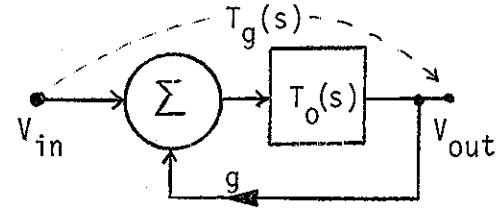


Fig. 5-10

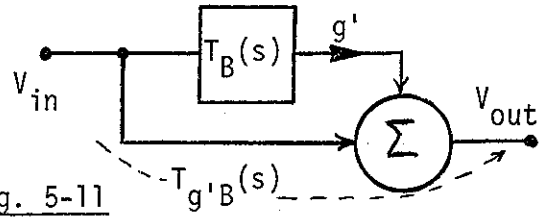


Fig. 5-11

by considering what happens when feedback is placed around a transfer function, as in Fig. 5-10. We can easily obtain the transfer function with a feedback gain g, $T_g(s)$ as:

$$T_g(s) = \frac{V_{out}}{V_{in}} = \frac{T_o(s)}{1 - gT_o(s)} \tag{5-33}$$

In the case where $T_o(s)$ is a general bandpass filter, $T_B(s)$ given by:

$$T_B(s) = \frac{As\omega_o}{s^2 + (\omega_o/Q_o)s + \omega_o^2} \tag{5-34}$$

then $T_g(s)$ comes out as:

$$T_g(s) = \frac{As\omega_o}{s^2 + \omega_o\left(\frac{1}{Q_o} - gA\right)s + \omega_o^2} \tag{5-35}$$

from which we see that the Q is now:

$$Q = Q_o/(1 - gAQ_o) \tag{5-36}$$

so Q is increased from its original value of Q_o if g is positive, and can be decreased if g is negative. Note that the feedback in the Deliyannis filter is positive.

As our second important case, we look at the "feed-forward" case where a=0, but where K is non-zero. This can be accomplished as in Fig. 5-9, where $K = R_4/(R_3+R_4)$. In this case, $T_t(s)$ from equation (5-29) becomes:

$$T_t(s) = K + T(s)[1-K] \tag{5-37}$$

and in the case of the MFIG bandpass $T_b(s)$ for T(s), we have:

$$T_K(s) = K\,\frac{s^2 + \frac{2s}{BRC}\left[\frac{2K + BK - B}{2K}\right] + 1/BR^2C^2}{s^2 + 2s/BRC + 1/BR^2C^2} \tag{5-38}$$

This has left the denominator unchanged, but has added a numerator which is the same as the denominator, except for the middle term (power of s). Note however that we can control this middle term by adjusting K. Our most interesting cases here are the notch filter that is obtained by making the middle term 0, and the all-pass which is obtained by making the middle term -2s/BRC. The notch is obtained when 2K+BK-B=0 or when:

$$K_N = B/(B+2) \tag{5-39}$$

and the all-pass is obtained when (2K+BK-B)/2K = -1, or when:

$$K_A = B/(B+4) \tag{5-40}$$

As was the case with the feedback, the all-pass and the notch here are specific examples of a more general principle of subtracting a bandpass from unity. Fig. 5-11 shows the setup of the general case, from which it can be shown that:

$$T_{g'B}(s) = g'T_B(s) + 1 = \frac{s^2 + \omega_o s[g'A+1/Q_o] + \omega_o^2}{s^2 + (\omega_o/Q_o)s + \omega_o^2} \qquad (5\text{-}41)$$

for which we get a notch for a value of g' equal to g'_N where:

$$g'_N = -1/AQ_o \qquad (5\text{-}42)$$

and we get an all-pass for a value of g' equal to g'_A where:

$$g'_A = -2/AQ_o \qquad (5\text{-}43)$$

This result makes sense in that it takes a certain gain to cancel the middle term, and twice that gain to change the sign of the middle term. The method of achieving useful notch and all-pass responses by controlling the middle term was first mentioned in Chapter 4, and will again be seen in the Biquad methods of Chapter 6.

5-3 LADDER NETWORK REALIZATION USING COMPONENT SIMULATION:

Over the years it has been well-established that the passive ladder structure has very low component sensitivity. This means that even when we get a component with poor tolerance, the resulting filter may still come out satisfactorily close to nominal. It thus makes sense to think of simulating or emulating the ladder structure. Two ways of doing this have proven useful and become popular. In this section, we will look at component simulation methods, where unwanted inductors are replaced by active R-C networks. In Chapter 6, a second method, that of simulating the flow graph of the ladder, will be examined. We will be using the same passive 3rd-order R-L-C low-pass for both cases.

We have already seen an example where an inductor was simulated: the active notch filter in Section 4-2. Here we will be doing things in a similar but more general manner, and will postulate the existance of a new type of circuit element called the "Gyrator." The gyrator is a four terminal network or "conversion box". We attach a capacitor to two of the terminals, and the other two look like an inductor. Fig. 5-12 shows our starting R-L-C passive network, and Fig. 5-13 shows the way a gyrator could be used to get rid of the inductor. Gyrators are not something we get off the shelf in a stockroom, but rather a circuit idea that we must realize. Below we will develop a circuit for a gyrator that can be used to simulate a grounded inductor (not a floating one as in Fig. 5-13). We will then see that a similar concept can lead to what is called a Frequency-Dependent Negative Resistor (or FDNR), which can be used to handle the fTloating inductor problem. Incidentally, the FDNR is also known by the more colorful name of "supercapacitor."

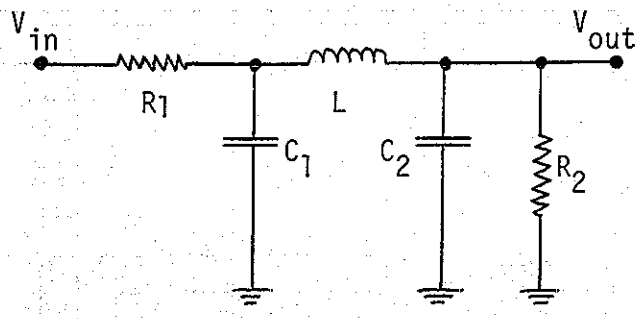


Fig. 5-12 R-L-C ladder for a third-order low-pass

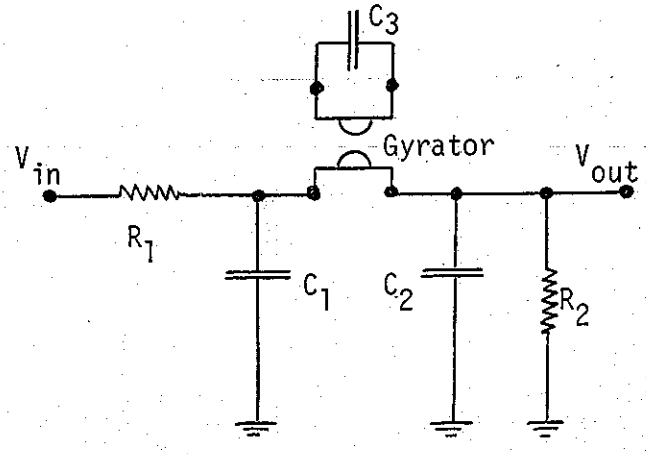


Fig. 5-13 Replacement of an inductor with a gyrator and a capacitor

The analysis of Fig. 5-12 is not difficult, being a matter of network analysis and persistence, and will not be done here. In Section 6-4, the network equations are written down, there because they are needed for the flow graph. The transfer function of Fig. 5-12 is:

$$T(s) = \frac{1/C_1C_2R_1L}{s^3 + s^2\frac{(C_1R_1 + C_2R_2)}{R_1R_2C_1C_2} + s\frac{[L + R_1R_2(C_1+C_2)]}{R_1R_2C_1C_2\,L} + \frac{R_1+R_2}{R_1R_2C_1C_2L}} \qquad (5\text{-}44)$$

This is a third order low-pass, and for example, if $R_1=R_2=1$, $C_1=C_2=1$, and $L=2$, we have a third-order Butterworth. The tabulation of element values for this structure and for many other passive R-L-C filters was a mainstay of filter research for many years, so there is no need to derive new data, if we choose to use this ladder approach. Here however we are interested in getting rid of the inductors, so the idea is to use the available element values, but to simulate inconvenient components.

Fig. 5-14 and Fig. 5-15 show two similar-looking circuits. The first of these simulates an inductor, and the second is the so-called FDNR or "supercapacitor." It will turn out that the supercapacitor will be needed to handle Fig. 5-12, while the simulated inductor or "Gyrator" of Fig. 5-14 will prove useful when we have grounded inductors, as we would for example, with a high-pass ladder (Fig. 5-16).

The analysis of Fig. 5-14, the gyrator, is much simpler than it might first appear. The network falls apart once we recognize that by the ideal op-amp principle, $V_1 = V_3 = V_5$. Then since I_3 must be flowing through both the lower R resistors, $V_4 = 2V_1$. Thus $I_2 = V_1/R$ as well, and this current also flows up through the capacitor C, from a voltage $V_3 = V_1$, producing V_2 as:

$$V_2 = V_3 - I_2/sC = V_1 - V_1/sCR = V_1(1 - 1/sCR) \qquad (5\text{-}45)$$

from which we get I_1 as:

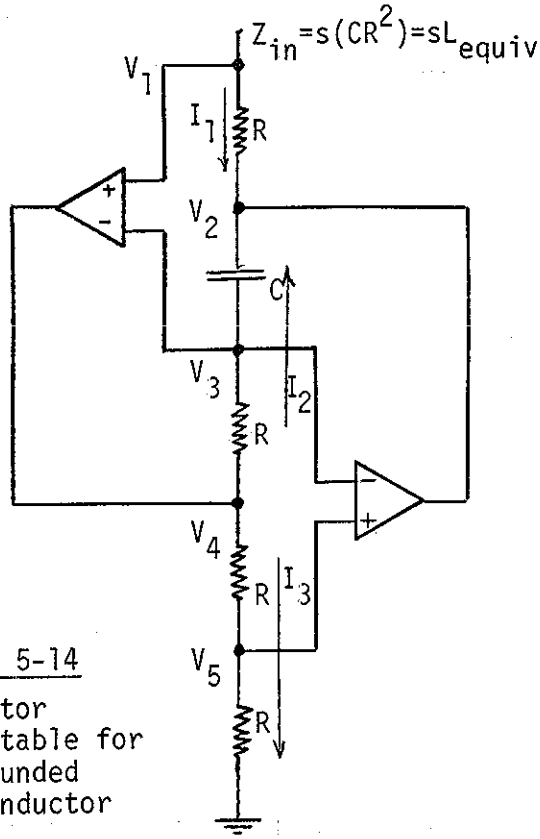


Fig. 5-14
Gyrator Suitable for grounded inductor

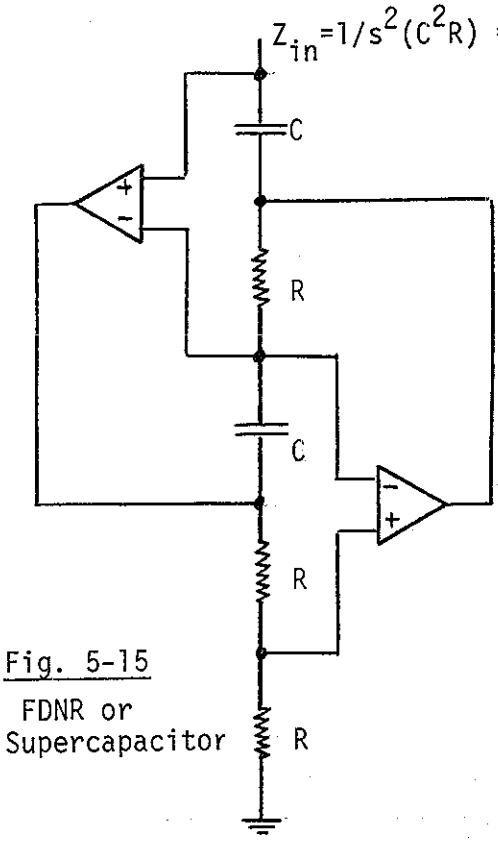


Fig. 5-15
FDNR or Supercapacitor

$$I_1 = (V_1-V_2)/R = (V_1 - V_1 + V_1/sCR)/R = V_1/sCR^2 \qquad (5\text{-}46)$$

Knowing V_1 and I_1 we now know the input impedance of the network at V_1, which is:

$$Z_{in} = V_1/I_1 = sCR^2 \qquad (5\text{-}47)$$

This impedance, being proportional to s, is inductive, so the circuit looks like an inductor to ground, with equivalent inductance:

$$L_{equiv} = CR^2 \qquad (5\text{-}48)$$

A very similar analysis gives the input impedance of Fig. 5-15 as:

$$Z_{in} = 1/s^2(C^2R) \qquad (5\text{-}49)$$

The impedance of equation (5-49) is one which we have not seen before, since it is proportional to $1/s^2$, and we have only seen impedances proportional to s (inductors), to s^0 (resistors), and to 1/s (capacitors). Being proportional to $1/s^2$, we can begin to understand the terminology "supercapacitor." Further, if we evaluate the impedance at $s=j\omega$, we get:

$$Z_{in}(j\omega) = -1/\omega^2C^2R \qquad (5\text{-}50)$$

which is negative and frequency dependent, hence the FDNR name.

The gyrator of Fig. 5-14 can be immediately applied to the high-pass ladder of Fig. 5-16, for example, with no complications, one gyrator for each of the two inductors. Realizing a floating inductor, as in the low-pass of Fig. 5-12 is more complicated. Gyrator circuits for floating inductors are possible, but are not efficient, relative to what can be done with the FDNR.

The FDNR idea is approached by asking what happens when all the network impedances are divided by s. Effectively, resistors R go to R/s = 1/s(1/R), so look like "capacitors" of value 1/R. Inductors with their impedance sL now look purely resistive with "resistance" L. Capacitors with their impedance 1/sC go to $1/s^2C$, which is our "supercapacitor" $1/s^2D$, with D=C. Note that this is not the same thing as dividing the components themselves by s. For resistors and inductors, the impedance is proportional to the component values, but not for capacitors, for which the impedance is inversely proportional to the component value. Thus by dividing all impedances by s, we are effectively dividing all resistors and inductors by s, but multiplying all capacitors by s. This leaves an R-L-C transfer function unchanged, as can be verified by equation (5-44), for example. We thus effectively "banish" inductors out of existence, at the price of having to come up with a new circuit element, the FDNR. We can not go out and buy an FDNR, but we know how to simulate one.

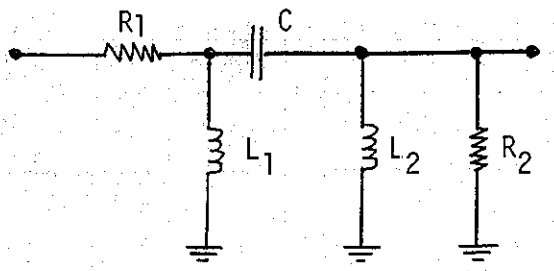


Fig. 5-16 3rd-Order High-Pass can make use of Gyrator of Fig. 5-14 to realize the inductors to ground.

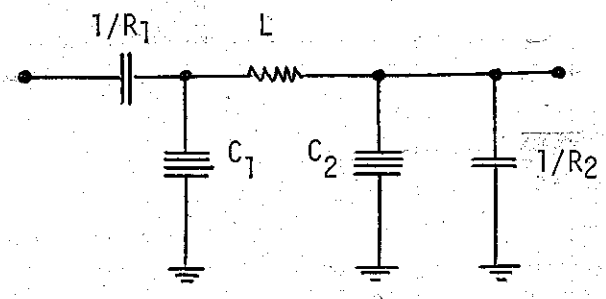


Fig. 5-17 FDNR transformation of Fig. 5-12 makes possible the low-pass using the "Supercapacitor", Fig. 5-15.

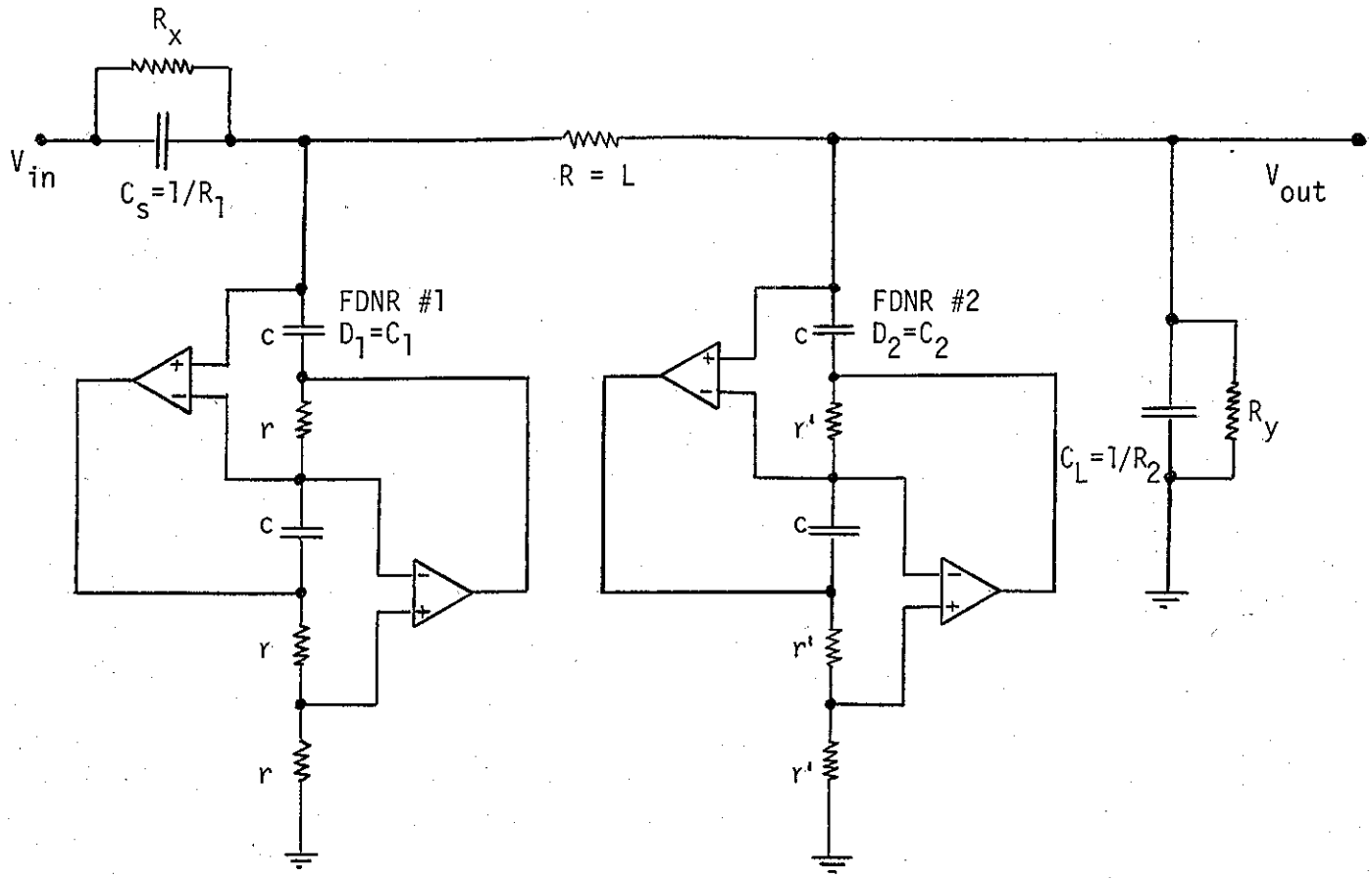


Fig. 5-18 FDNR realization according to Fig. 5-17, ultimately realizing the 3rd-order Low-Pass of Fig. 5-12

Fig. 5-18 shows a realization using the FDNR method. Essentially we start with the known passive R-L-C prototype (Fig. 5-12), convert it using the FDNR (Fig. 5-17), and then place the FDNR realization of Fig. 5-15 into Fig. 5-17, arriving at Fig. 5-18. Note that any differences between the FDNR values (corresponding to difference between C1 and C2), are represented here by the use of a resistor r in one, and a resistor r' in the other. (In practice, there are numerous ways to "tune" the FDNR.) Aside from that, the only unexpected components are the resistors Rx and Ry which are needed to supply bias current to the op-amps, in a manner to be explained later.

In working out the component values, the important thing to keep in mind is that it is Fig. 5-18 that must have components in a practical range. The components need not be practical in the prototype of Fig. 5-12. In theory, we can scale the network either in the prototype, or in the FDNR realization, but it is usually easiest to do in the prototype. Accordingly we must keep in mind that Cs and CL are the reciprocals or R1 and R_2 respectively, and that R is numerically equal to L. The supercapacitors D_1 and D_2 are given by:

$$D_1 = c^2 r \tag{5-51}$$

and:

$$D_2 = c^2 r' \tag{5-52}$$

and are numerically equal to C_1 and C_2 respectively.

Resistors R_x and R_y have been added to the circuit with two things in mind. First, they are necessary to provide the very small bias currents that the op-amp inputs require. Without these, the (+) inputs of the upper op-amps would be dc isolated, and the bias currents would charge the capacitors to power supply limits. In fact, only one of R_x or R_y is required to supply bias current, and with good quality op-amps such as BiFET types, the currents are very small so that very large resistors (high MegOhm range) could be used with negligable effect on the rest of the circuit.

However, once we find it necessary to have either R_X or R_Y, it becomes necessary to have them both, and once one is chosen, the value for the other is determined as well. It all has to do with maintaining the correct DC gain. The dc gain of the passive prototype of Fig. 5-12 is $R_2/(R_1+R_2)$, since the capacitors become charged, and the current through the inductor becomes constant. Below we will show that at dc, no current flows into the FDNR's. [For the moment, this should be true from equation (5-50) since the impedance is infinite at dc.] In this case, the dc gain of Fig. 5-18 is seen to be $R_Y/(R_X + R + R_Y)$. If we set these dc gains equal:

$$R_2/(R_1+R_2) = R_Y/(R_X + R + R_Y) \qquad (5\text{-}53)$$

we can choose R_X or R_Y large and arbitrary, and calculate the other.

In this view, R_X and R_Y are not chosen to set the dc gain, but rather to maintain it at the value it should have. Consider what the dc gain of Fig. 1-18 would be without R_X and R_Y (ignore the bias currents as well). It may not even be clear that Fig. 5-18 has a non-zero dc gain, since it might seem that the capacitor C_S "blocks" dc. In actual fact however, while a capacitor "blocks" dc current, it is perfectly capable of holding a dc voltage. Once dc is applied, after sufficient time passes, an amount of charge q has flowed from V_{in}, charging both C_S and C_L to voltages q/C_S and q/C_L respectively, such that:

$$V_{in} = q/C_S + q/C_L \qquad (5\text{-}54)$$

(Since current has stopped, or at least become negligably small, there is no remaining voltage drop across R.) However, V_{out} is also the voltage on C_L, which is q/C_L, so

$$\text{dc gain} = V_{out}/V_{in} = C_S/(C_S+C_L) \qquad (5\text{-}55)$$

Since $C_S = 1/R_1$ and $C_L = 1/R_2$, equation (5-55) is in agreement with the dc gain of the passive network being $R_2/(R_1+R_2)$.

What remains to be shown is that there is no current flowing into the FDNR's. This we discussed from the impedance point of view of equation (5-50), but we can also see it physically. Looking at one of the FDNR's, the only possible current path into the FDNR is through the upper of the c capacitors to the lower op-amp output. (This is because the (+) input of the upper op-amp of course draws no current, and because the output of the lower op-amp absolutely determines the voltage at the bottom of the capacitor - nothing below makes any difference.) Now, considering dc, no current can be passing through the upper c, and hence no current enters the FDNR.

CHAPTER 6

INTEGRATOR BASED DESIGNS

6-1 INTEGRATORS - IN GENERAL AND IN PARTICULAR:

An integrator is not a filter, although it may be used as part of a filter. Integrator-based filter design methods include the very popular "state-variable" approach and the "flow-graph simulation" approach which offers excellent sensitivity properties. These approaches use the fact that the integrator is a multiplication by 1/s. Before studying these approaches, we need to understand the integrator by itself.

An integrator has a transfer function that goes as 1/s, so to keep the units correct, it must have a time constant, which we conveniently write as RC, since we often relate it directly to network components. Accordingly, our integrator transfer function looks like:

$$T(s) = 1/sCR \qquad (6\text{-}1)$$

It is clear that this has a pole at s=0, which is not in the left half-plane, so the integrator is not, by itself, stable. It will be useful at this point to look at an example of an integrator circuit, which is shown in Fig. 6-1a. This is a very popular inverting integrator structure, which is one of the possible generalizations of the inverting amplifier structure (Fig. 1-14). The transfer function is obtained as the negative of the impedance in the feedback leg divided by the impedance in the input leg, or:

$$T(s) = -(1/sC)/R = -1/sCR \qquad (6\text{-}2)$$

which is an inverting version of equation (6-1). (If we need a non-inverting integrator, we could at least just add an op-amp inverter to Fig. 6-1a, although there are alternatives which we will discuss.) We can understand why this is called an integrator based on our experience with Laplace transform. Alternatively, we can see by example (Fig. 6-1b) how the circuit responds to a particular time waveform. In Fig. 6-1b, we show a rectangular pulse arriving at the input of our integrator, and we assume that the integrator's output is zero before arrival. When the pulse arrives, a current V_p/R begins flowing into the op-amp summing node (the - input with the + input grounded). This current has no place to go, except out through the capacitor, and the output voltage accordingly ramps (downward) at a rate:

$$dV_{out}/dt = i/C = V_p/RC \qquad (6\text{-}3)$$

from which we can infer the integrating capability of the circuit. Note that when the pulse ends, the current stops, and the output holds at -Vptp/RC. In particular, it does not reset to zero. Accordingly we also have the idea that the past history of the integrator comes into play (the "arbitrary constant" added to integrals).

Having taken a brief look at the time response of the integrator, we know from the transfer function that in the frequency domain, there is a pole at s=0, and the frequency response is:

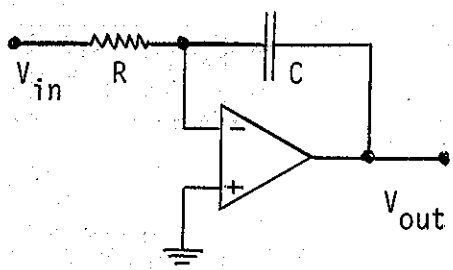


Fig. 6-1a The inverting integrator

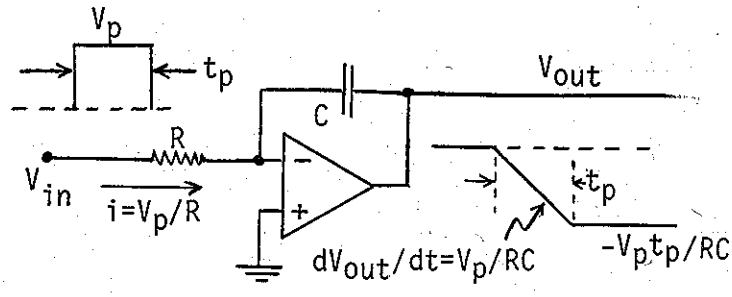


Fig. 6-1b Response of inverting integrator to an input pulse.

$$|T(s)| = 1/\omega RC \qquad (6\text{-}4)$$

From this we see that the response blows up at dc, which is the same fact that the pole at s=0 was telling us. It is instructive to consider a plot of the frequency response on log-log paper, which gives a $1/\omega$ roll-off, which is a 45° downward angle. Since log-log paper "goes on forever" in all directions, so does this response curve, as suggested in Fig. 6-2b. The importance of this is, in addition to calling attention to the instability at zero frequency, that there is no break point or "characteristic frequency" on this curve. Correspondingly, as we shall discuss in more detail below, there is no real absolute meaning to the integrator's so-called time constant. Note however that the integrator's response is the high-frequency limiting case of the first-order low-pass filter $T(s) = 1/(1+sCR)$.

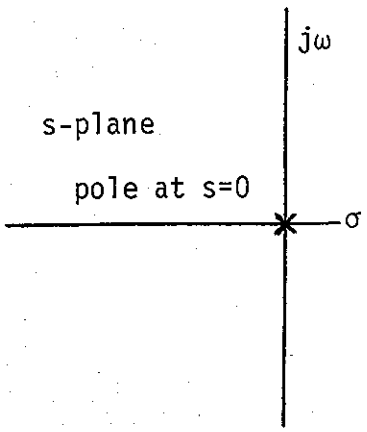


Fig. 6-2a Pole of integrator at s=0 in s-plane

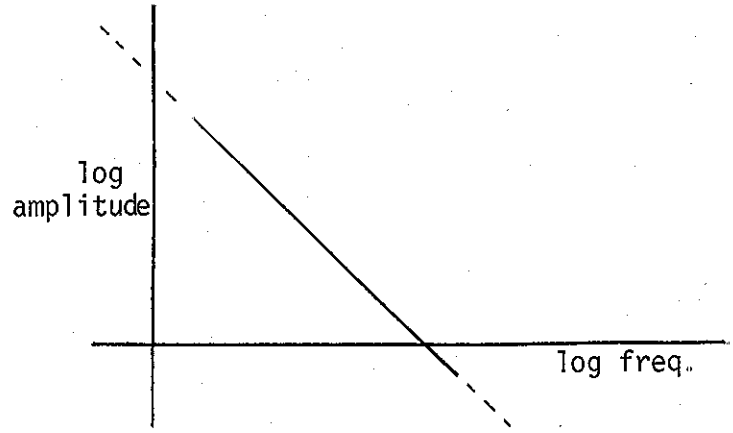


Fig. 6-2b "Frequency Response" of integrator is 45° slope on a log-log plot.

At this point, we will attempt to put together some of these facts which we have discovered concerning the integrator, and to put the really significant points about the integrator in proper perspective. The first of these points is that the integrator (all integrators) are unstable, unless they are stabilized. Exactly what does the pole at s=0 mean? The pole at s=0 is on the jω-axis, and accordingly, it represents an oscillator at the corresponding frequency ω, which is ω=0. Thus we have an oscillator at zero frequency, which is a "dc oscillator." Like all oscillators with first-order poles on the jω-axis, in theory, oscillation does not begin until some non-zero excitation starts it off. As we saw in Fig. 6-1b, the integrator's output was zero until a pulse arrived, which caused it to ramp. Now that the oscillator has been excited, it continues to oscillate (continues to output a dc voltage of $V_p t_p/RC$).

The problem here is that in a real case there are always at least some small dc offset voltages in our circuits, and these are enough, at the input of integrators, to cause the integrator to drift around, and eventually pin at the power supply. (In fact, an integrator formed from a real op-amp will integrate its own offset voltage, even if the input resistor is grounded.) What do we do about this?

Our first thought is to somehow "damp" the integrator. Intuitively we see that the instability is a matter of the capacitor charging up, and we might suppose that if we put a very large resistor across the capacitor, it might drain off this excess charge, and might be large enough to not affect the performance much otherwise. This is a common practice, and we can understand it in terms of pole placement. We might suppose that if a pole at exactly s=0 is a problem, we might be able to back it off ever so slightly into the left half-plane, and still have something that looks like an integrator in our application. The so-called "damping" resistor across the integrator's capacitor does precisely this: the pole moves into the left half plane, and just barely in if the resistor is of a very high value.

Fig. 6-3

Undamped Integrator $T_i(s)$ and Damped Integrator $T_{id}(s)$

$T_{id}(s)$ is an inverting version of our familiar first-order low-pass if $r = R$.

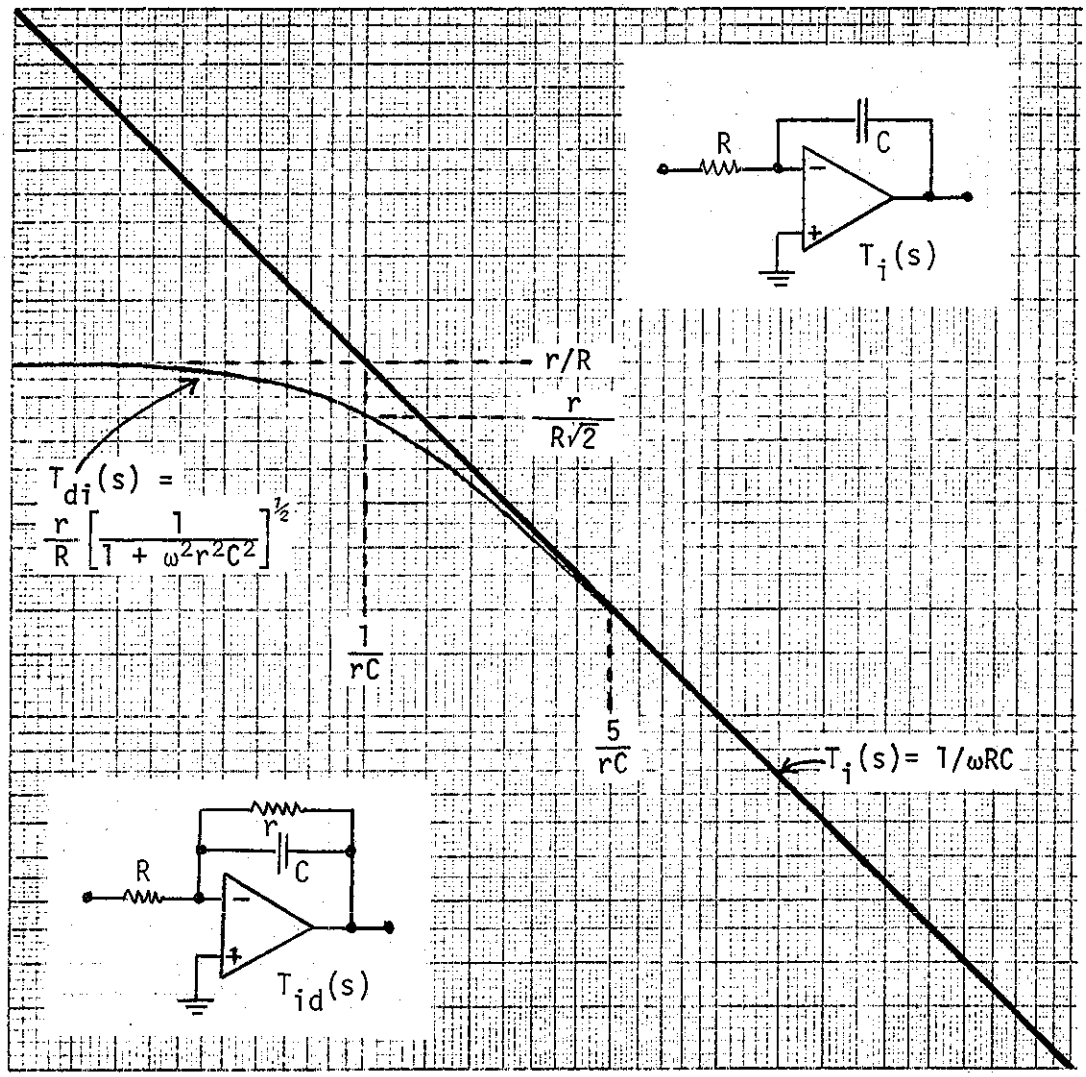


Fig. 6-3 compares the damped and the undamped integrators. We note of course that a single real pole in the left half-plane is exactly a first-order low-pass filter, so a damped integrator and a first-order low-pass are mathematically virtually identical. In fact, the transfer function for the damped integrator is:

$$T_{id}(s) = \frac{-r/R}{1 + sCr} \qquad (6\text{-}5)$$

so if r=R, the damped integrator is an inverting version of our familiar first-order low-pass. The difference is more in that with the damped integrator, r is thought to be much larger than R. By taking the dc limit of equation (6-5), letting s=0, we see that this means that the DC gain is large: -r/R. (Note that we can also get the dc gain simply by observing that the circuit becomes an inverting amplifier with gain -r/R at dc, where C is effectively removed from the circuit.) Thus the undamped integrator continues up to an infinite response at dc, while the damped integrator (first-order low-pass) curves away and levels off at a magnitude r/R. From Fig. 6-3 we note that as a guide, the two curves are pretty much the same for frequencies of 5/rC and higher. This is why a damped integrator can be used as a true integrator for high-enough frequencies.

Not all integrators used in practice must be damped in this obvious manner however. Integrators may be effectively stabilized by placement in overall loop structures, of which the state-variable filter that we are leading up to is a well-known example. In some other analog circuits, other means of damping or "reset"

will be seen, but these are outside of the study of linear circuits which we are concerned with here. Consequently, when an integrator is seen in a network, we must ask what it is that is stablizing it. Thus recognition that integrators are unstable until proven stable is our first important point.

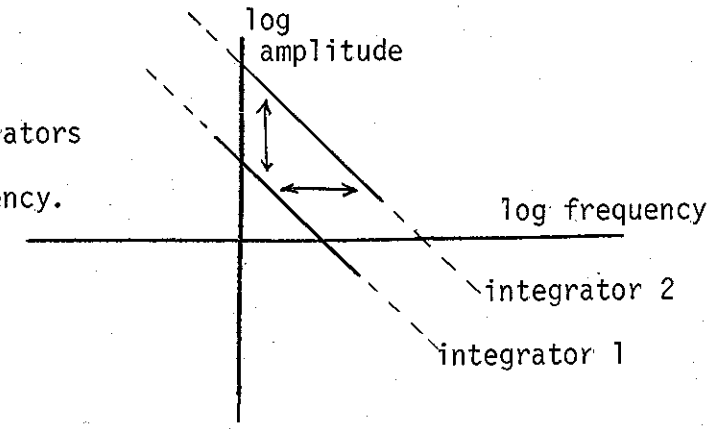
The second point relates to the lack of distinction between integrator time constant and integrator gain. Above we mentioned that there was no characteristic point on an integrator's frequency response curve - it was just a 45° line going on forever in both directions. We can look at this by considering Fig. 6-4 where we show two integrator curves on a log-log plot. If we ask how one curve could be obtained from the other, it is clear that we could use either an up-down move or a left-right move, or some combination, all with an equivalent result. An up-down move corresponds to a change of gain factor, while a left-right move corresponds to a change of time constant, and we see that these are equivalent. This would not be true with the first-order low-pass, for example, where a change of time constant would change the cutoff frequency. Another way to make the same point is to suggest, for example, a gain factor of 2 be applied to equation (6-1), which would give:

$$T(s) = 2/sCR = 1/sC(R/2) \qquad (6\text{-}6)$$

from which we see that a gain of 2 is equivalent to cutting the time constant in half. This also makes sense in the time domain. If we consider Fig. 6-1b with R replaced by R/2, the output would go twice as high as it did, which is a gain factor of 2.

Fig. 6-4

Two different integrators differ equivalently in gain or in frequency.

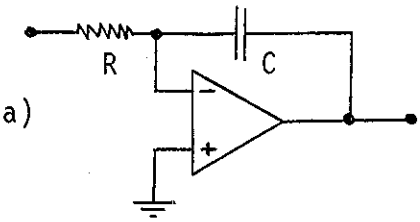


A third point relates to the conditions under which the output of an integrator can be a constant. Clearly for such a case, the input must be held at zero. This of course means that if the output of an integrator is held at zero, its input must be zero. This observation can often greatly simplify analysis of the dc gain of filters using integrators. Under dc conditions, all points in the filter must be dc (constants) and this in turn forces all integrator inputs to be zero (or a net of zero if there are multiple inputs).

With the above points in mind, we can go on to consider possible realizations of integrators, and Fig. 6-5 summarizes the better-known integrators and integrator-related circuits. Fig. 6-5a is the best known and the simplest, the inverting integrator. Fig. 6-5b is our well-studied first-order low-pass. As we have discussed, this circuit looks like an integrator at high enough frequencies. (In fact, in some older references, this is called an integrator.) Fig. 6-5c is the damped integrator which we have also studied above, and we see how this also resembles a perfect integrator at some high enough frequencies. Also as we mentioned, Fig. 6-5d gives an inverting form of the first-order low-pass.

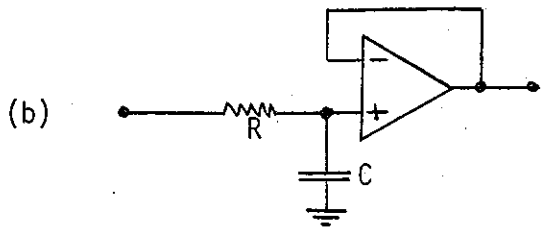
Fig. 6-5 Integrator and Integrator-Related Circuit Collection

Inverting Integrator



$T(s) = -1/sCR$

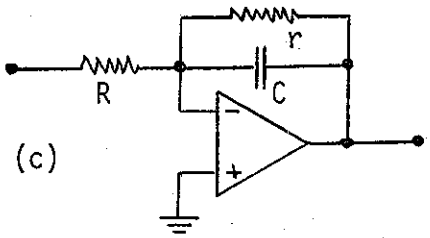
First-Order Low-Pass



$T(s) = 1/(1+sCR)$

$\simeq 1/sCR$ for high frequencies

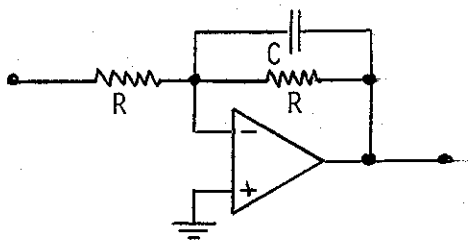
Damped Integrator



$$T(s) = \frac{-r/R}{1+sCr}$$

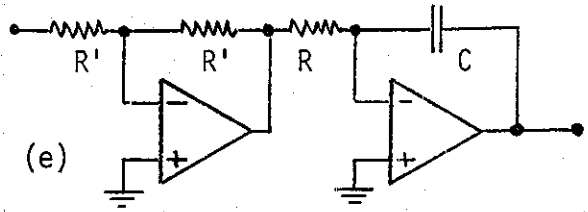
$\simeq 1/sCR$ for high frequencies

Inverting First-Order Low-Pass



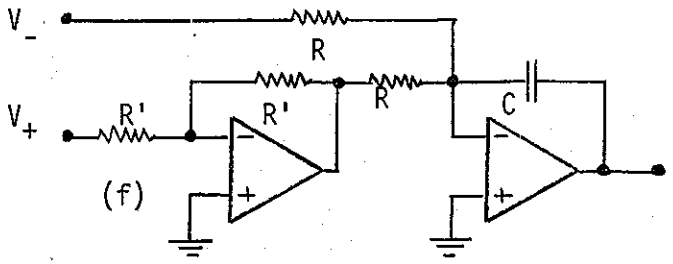
$T(s) = -1/(1+sCR)$

Non-Inverting Integrator



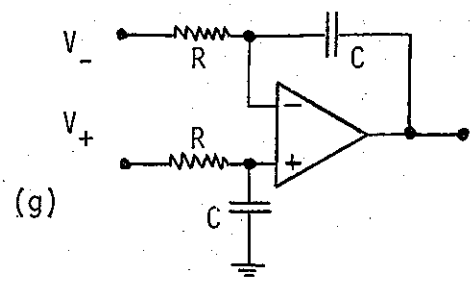
$T(s) = 1/sCR$

Differential Integrator



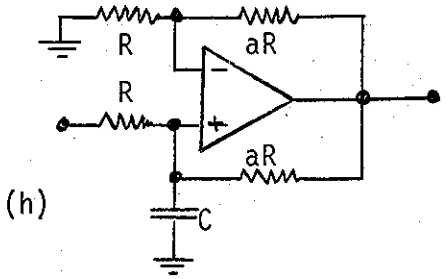
$T(s) = V_{out}/(V_+ - V_-) = 1/sCR$

Differential Integrator
(two caps)



$T(s) = V_{out}/(V_+ - V_-) = 1/sCR$

Non-Inverting Integrator
(Generalized Deboo)



$T(s) = (1+a)/sCR$

The lower portion of Fig. 6-5 relates to the need for non-inverting integrators and for differential integrators. Note that if we have a differential integrator, we can always make it a non-inverting integrator by just grounding the (-) input and using only the (+) input. Fig. 6-5e shows a simple idea about obtaining a non-inverting integrator from the inverting one - just add on an inverting stage. This inverter need not use resistors R, which is why we denote them by R', a value of convenience. It is also true that the inverting stage could follow the integrator. Here we have put it first so that it more easily converts to the differential integrator of Fig. 6-5f. Here we have used the idea that the (-) input of the integrator op-amp is a summing node, so we can just put back an inverting input on Fig. 6-5e. Here both the resistors marked R must be the same, unless a weighted summation is needed. (In such a case, one might suppose that the two inputs would have different time constants, but the remark about the interrelationship between gain and time constant should be kept in mind.). It will turn out that neither Fig. 8-5e or 8-5f is a particularly good idea if we are at all concerned with the effects of real op-amps at high frequencies (see next chapter). However, both offer simple and usable circuits at lower frequencies.

Fig. 6-5g is an alternative approach to a differential integrator. Note that this one uses two capacitors, while its competitor Fig. 6-5f uses one capacitor but two op-amps. In deciding which is better, one should keep in mind that capacitors may be more expensive, and perhaps larger than op-amps. Finally, Fig. 6-5h offers a non-inverting integrator with only one capacitor, and with some "gain" if desired. The circuit is interesting in that there is a 50-50 chance that due to resistor tolerance, it may already be damped, even though it is not damped intentionally (see problems at end of chapter).

We now have a good idea what integrators are, and have examined some important points with regard to stability and gain/time-constants. We have also looked at some practical circuits. Once we go over to considering real instead of ideal op-amps, we will find that integrators often have serious limitations at higher frequencies. The beauty of it though (see next chapter) is that we can fix or "compensate" our circuits so that they look much more ideal. Thus we can go ahead with integrator based filter design with confidence that we can arrive at some excellent practical circuits.

6-2 THE STATE-VARIABLE FILTER AND RELATED STRUCTURES:

We have in mind that a state-variable filter is a configuration of a summer and two integrators in series, with feedback from the integrators to the summer. This particular configuration offers us low-pass, bandpass, and high-pass outputs (with others available), and typically uses three, four, or possibly five op-amps in the attempt. Fig 6-6a shows the usual configuration in block form. The integrators are represented by 1/s, and we have feedback paths of -1 and -1/Q as shown. The three internal voltage sources are denoted V_H, V_B, and V_L in anticipation of the eventual transfer functions at these points.

The analysis of all state-variable filters is much the same, whether they are in block form, or as one of the configurations using op-amps which are also shown in Fig. 6-6. We will begin with the block form, and find the voltage V_H, which is the output of the summer:

$$V_H = V_{in} - (1/Q)V_B - V_L \qquad (6\text{-}7)$$

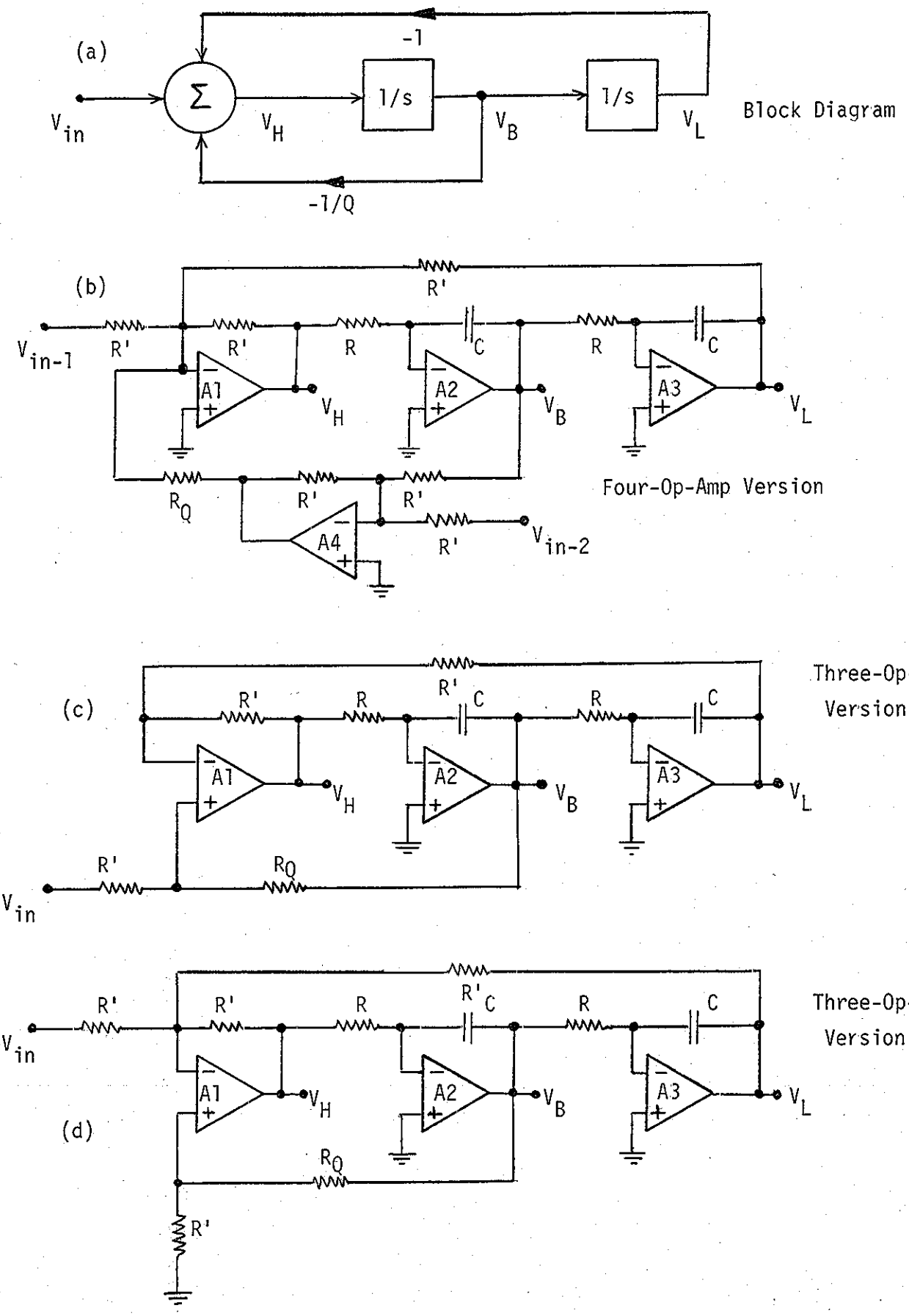
Next we note that the relationship between V_B and V_H, or between V_L and V_B, is a matter of a single integration (multiplication by 1/s), and we can write:

$$V_B = V_H/s \qquad (6\text{-}8)$$

and

$$V_L = V_B/s = V_H/s^2 \qquad (6\text{-}9)$$

Fig. 6-6 Basic State-Variable Filter and Some Standard Configurations



We can substitute equations (6-8) and (6-9) back into equation (6-7), and then solve for the transfer function:

$$T_H(s) = V_H/V_{in} = \frac{s^2}{s^2 + (1/Q)s + 1} \qquad (6\text{-}10)$$

which is a nice second-order high-pass response. Again applying equations (6-8) and (6-9), we can get the transfer functions at V_B and V_L as:

$$T_B(s) = V_B/V_{in} = \frac{s}{s^2 + (1/Q)s + 1} \qquad (6\text{-}11)$$

which is bandpass, and

$$T_L(s) = V_L/V_{in} = \frac{1}{s^2 + (1/Q)s + 1} \qquad (6\text{-}12)$$

which is low-pass.

From these results we see that we have a "three for one" filter. Even more so, we can do a weighted sum to obtain an arbitrary numerator as:

$$T(s) = \frac{As^2 + Bs + C}{s^2 + (1/Q)s + 1} \qquad (6\text{-}13)$$

Equation (6-13) is quadratic in both the numerator and the denominator, and is accordingly referred to as "Biquadratic." In general, structures which are capable of realizing a biquadratic transfer function are called "Biquads," and the state-variable filter here may be called a biquad (there are others).

The analysis of the block diagram has shown us several things. First, we got three different transfer functions, all with the same denominator however. We note that the path we called -1/Q, from the bandpass back to the high-pass, has appeared in the transfer function exactly where we want "Q" to appear. Thus the Q of the filter is the reciprocal of the gain from the bandpass back to the high-pass. This can be a useful shortcut in analysis if we do it correctly. Also, we did take a shortcut by using 1/s instead of 1/sCR here, but it is clear how the integrator time constant could be put back into the transfer functions, in each term, so that the units are correct.

The three configurations of op-amps in Fig. 6-6b, c, and d are examples of how state-variable filters can be realized. Because the node voltages V_H, V_B, and V_L are all related by the inverting integrator used (-1/sCR), analysis is not as involved as it might first appear. Fig. 6-6b is the simplest because it uses an extra op-amp to simplify the summer. The problem comes in when we consider that the feedback paths are both negative ones, which suggests that the op-amp inverting summer would be ideal here. However, we are employing inverting integrators. The double inversion cancels when we go from V_H all the way to V_L, but V_B is inverted, which is the reason the fourth op-amp (A4) is used. At this point, Fig. 6-6b resembles Fig. 6-6a very closely. We can observe that the gain across A4 is -1, while that across A1, from A4, is $-R'/R_Q$, for a gain from VB to V_H of R'/R_Q. This means that the Q, which is the reciprocal of this gain, is given by:

$$Q = R_Q/R' \qquad (6\text{-}14)$$

which is a nice simple result. (Note that the extra inversion needed to make this negative feedback came from the inverting integrator A2.) We can then put the RC time constant back into the integrators, and write down the correct transfer functions, for example:

$$T_B(s) = V_B/V_{in\text{-}1} = \frac{s/RC}{s^2 + (R'/R_Q)\frac{s}{RC} + 1/R^2C^2} \qquad (6\text{-}15)$$

Here we could have chosen any of the transfer functions, but we chose the bandpass because we want to look at the peak gain, and we know how to do that easily (as we did for equation (3-55)). The peak gain comes out R_Q/R'. We may often want to have a variable Q bandpass using the state-variable, and if we try to do this, we get a variable gain as well, since changing R_Q affects both. However, this is the purpose of the second input point in Fig. 6-6b. If we use the point V_{in-2} instead of V_{in-1}, then the input is subject to the gain factor R'/R_Q, exactly as was the Q-determining gain from V_B to V_H. This factor R'/R_Q would be added to the transfer functions, and in the case of equation (6-15), it exactly cancels the peak gain of R_Q/R', resulting in a unity gain bandpass at all values of Q. Accordingly, Fig. 6-6b might be used for simplicity, but it is also useful in variable Q cases where we want fixed gain.

Fig. 6-6c and Fig. 6-6d shows two commonly seen state-variable configurations which are somewhat similar. Both use only three op-amps instead of four, achieving the extra inversion of the bandpass by summing not on the summing node (-) of the op-amp summer, but rather on the (+) input. This complicates the summation calculation somewhat. Some years ago, when op-amps were fairly expensive, it was important to save an op-amp when possible. Today, cost is not too important, but it may still be prudent to save an op-amp because each and every op-amp adds a pole of its own which complicates the analysis when high frequencies are involved (see next chapter). Both these configurations can be analyzed much as we have handled things above. We know what the integrators do, and we know how to set up the summer in the ideal case of $V_- = V_+$ for A1 in both cases. However, there are simpler ways which can lead to the correct results. This will involve finding the gain from V_B to V_H, establishing the Q, and finding the dc gain of the low-pass.

We can illustrate these procedures with Fig. 6-6c. To do this, we need to be clear on the "principle of superposition." The total voltage at V_H is the result of contributions from V_{in}, V_B, and V_L. We are interested in what part of V_B gets to V_H. Using the principle of superposition, we can set V_{in} and V_L to zero and just consider V_B. With V_{in} and V_L set to zero, the configuration around the summer is as seen in Fig. 6-7. The resistor R' that was going to V_L is now effectively grounded, as is the R' resistor that went to the input. The upper R' resistor now forms a non-inverting amplifier with gain of 2, from V_+ to V_H. At the bottom, we now have a voltage-divider from V_B to V_+, and the voltage V_+ is given by:

$$V_+ = V_B \frac{R'}{R'+R_Q} \tag{6-16}$$

and by the non-inverting amplifier result we have:

$$V_H = 2V_+ = \frac{2R'}{R'+R_Q} V_B \tag{6-17}$$

from which we see that Q is:

$$Q = (R'+R_Q)/2R' \tag{6-18}$$

Next we need to determine the dc gain of Fig. 6-6c. To do this, we assume that if some dc value is input, V_{in-o}, we get some dc output at the low-pass, V_{L-o}. Now, since V_{L-o} is a constant value, and because V_L is the output of an integrator, the

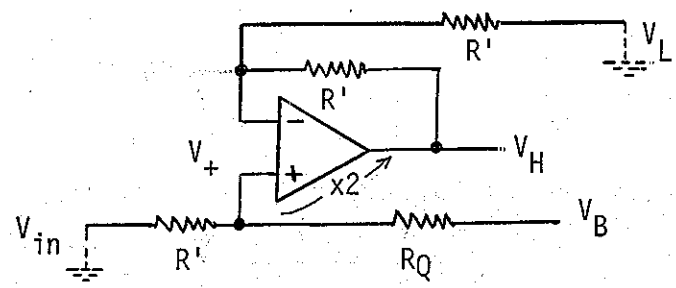


Fig. 6-7 Summer that is working to find gain from V_B to V_H

input to this integrator should be zero, or $V_B = 0$. (Incidentally, this tells us that the dc response of the bandpass is zero - something we already should have figured out.) Since V_B is zero, a perfectly good constant (and the output of integrator A2), it follows that V_H=0. (Again, the response of a high-pass to dc should be zero.) With $V_B = 0$, the (+) input of A1 is:

$$V_+ = V_{in-o} \frac{R_Q}{R'+R_Q} \tag{6-19}$$

and the (-) input of A1 should be:

$$V_- = V_{L-o}/2 \tag{6-20}$$

since V_H=0. For the ideal op-amp, $V_+ = V_-$, and we get, combining equations (6-19) and (6-20), for the dc gain:

$$\frac{V_{L-o}}{V_{in-o}} = \frac{2R_Q}{R'+R_Q} \tag{6-21}$$

Knowing the dc gain and the Q now, we can write down the low-pass transfer function for Fig. 6-6c as:

$$T_L(s) = \frac{\frac{2R_Q}{R'+R_Q}(1/R^2C^2)}{s^2 + \frac{2R'}{R'+R_Q}\frac{s}{RC} + 1/R^2C^2} \tag{6-22}$$

The other two transfer functions can then be obtained by multiplying up by -sCR.

Fig. 6-6d yields to the same sort of analysis, the details of which are left to the reader. In this case, a non-inverting gain of 3 is found from the V_+ terminal of A1 to V_H, so the Q is given by $(R'+R_Q)/3R'$. The dc gain is found to be -1 for this configuration, again simply arrived at using the "stalled integrator" method. In the same way, we can write down the transfer functions. For example, the high-pass has to be:

$$T_H(s) = \frac{-s^2}{s^2 + \frac{3R'}{R'+R_Q}\frac{s}{RC} + 1/R^2C^2} \tag{6-23}$$

Incidentally, these same results can be achieved the "hard way" by direct analysis.

6-3 VARIATIONS ON THE STATE-VARIABLE / BIQUAD THEME:

Having now worked with the basic state-variable structure, we can understand some useful variations, of which there are far more than we can begin to catalog here. First, by summing the high-pass and the low-pass, we can achieve a notch response. We can understand this as a zero placed on the jω-axis, due to the absence of a middle term (power of s) in the numerator. In this state-variable case, we can also understand it in terms of the 90° phase shift of the integrators. The integrator produces a 90° phase shift at all frequencies, which we can understand in terms of the pole at zero always being 90° around from from a line drawn out from a point on the jω-axis, parallel to the real axis. Accordingly, at the point where the low-pass and high-pass curves cross, the amplitudes will be the same, and because the low-pass and high-pass are "two integrations apart," they are 180° apart. Summing the signals results in cancellation, hence a notch.

All-pass networks are also easily achieved with a state-variable based design by proper choice of the summation weights in equation (6-13). For a notch, we generally would like A=1 and C=1 with B = -1/Q. Thus in achieving an all-pass, all three of the low-pass, bandpass, and high-pass should be properly summed, and

not just with the correct weight, but with the correct polarity. Note that with the state-variable filters using the inverting integrator, the bandpass node is fortuitously already inverted with respect to low-pass and high-pass, so a simple inverting summer can be used.

While we can always achieve a general biquadratic response through output summation, at times different useful responses can be achieved by inputting the signal into different input points, or to several points simultaneously. Fig. 6-8 shows one such possibility, which is an "input notch" type of network. The network looks very much like the ones we have already seen, except that the usual input point (input signal to the summer) is not used. Instead, the signal is input to two other points (the integrator summing nodes). Note that one of the input components is a capacitor, not a resistor. The result is that a notch response now appears where the bandpass did in previous examples. The transfer function is:

$$T_N(s) = \frac{s^2(C'/C) + (R/R'')/R^2C^2}{s^2 + \frac{2R'}{R'+R_Q}\frac{1}{RC}s + 1/R^2C^2} \qquad (6\text{-}24)$$

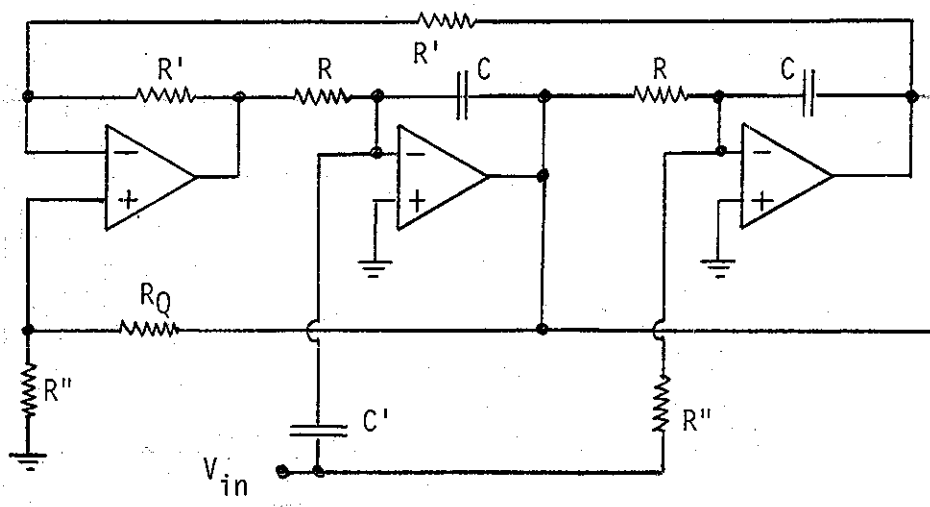


Fig. 6-8
Input Notch
(standard notch when C=C' and R"=R)

Probably the most familiar variation on the state-variable theme is a somewhat different circuit that is often mistaken for a state-variable. This circuit is also a "biquad" in the sense we have discussed above, but is also a "biquad" in the sense that this is the term that is often used to distinguish it from the state-variable filter. It is actually easy to tell the two apart. As we have said, the state variable has two integrators and a summer in a loop, with feedback from both integrators. (In fact, it is this feedback that stablizes the integrators overall.) The "biquad" consists of a summer, a damped integrator, and an undamped integrator in a loop. Generally, the summation is done on the input of the damped integrator, while at the same time an additional inverter is required in the loop. Fig. 6-9a shows the block version of such a "biquad" while Fig. 6-9b shows a three op-amp realization. Note the superficial resembalance of Fig. 6-9b to the configurations of Fig. 6-6 for example.

It is fairly easy to analyze the biquad of Fig. 6-9b by any number of procedures, and the transfer function can be obtained, as:

$$T_B(s) = V_B/V_{in} = \frac{-s/RC}{s^2 + (R/R_Q)(1/RC)s + 1/R^2C^2} \qquad (6\text{-}25)$$

which is a bandpass function. Note that this is integrated to a low-pass response at V_L, but that here, unlike the state-variable, there is no high-pass response. We can tell that there can only be two different responses because A2 provides only an inversion, and no new response of its own. Design equations are easily obtained from equation (6-25), and we note that the Q is simply controlled by the resistor R_Q, as $Q = R_Q/R$, which is simpler than the three op-amp circuits of Fig. 6-6c and Fig. 6-6d.

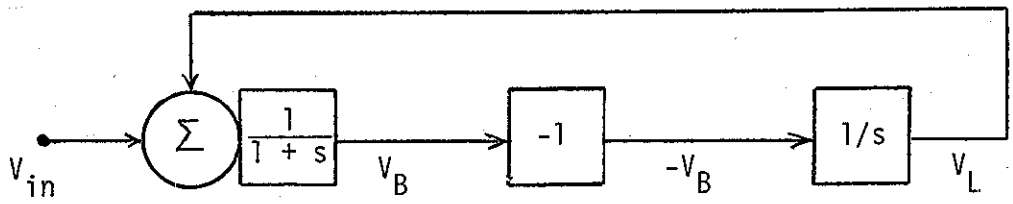


Fig. 6-9a

The "biquad" structure

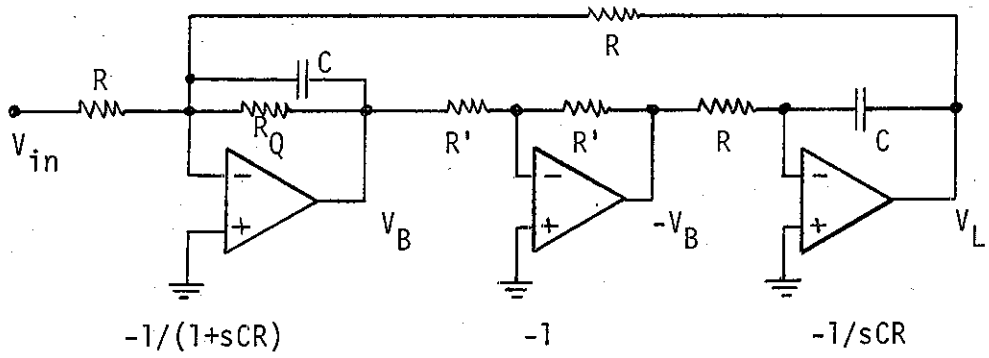


Fig. 6-9b

Realization of the "biquad"

The "biquad" approach may not be as restricted as it first appears, as after all, we may not be after all three responses simultaneously. Further, it is possible to have a "biquad" that has high-pass and bandpass instead of bandpass and low-pass, and this is left as an exercise to the reader (see problems at end of chapter). Another disadvantage that might be perceived is that in having only low-pass and bandpass or bandpass and high-pass, it is not possible to sum outputs for notch, for all-pass, or for a general biquadratic. However, in having the bandpass, we can achieve notch and all-pass by subtracting the bandpass from unity. To make this point, we can write:

$$T_{in}(s) = (V_{in}/V_{in}) = \frac{s^2 + (R/R_Q)(s/RC) + 1/R^2C^2}{s^2 + (R/R_Q)(s/RC) + 1/R^2C^2} = 1 \qquad (6\text{-}26)$$

This technique of subtracting a bandpass from unity is of course more general, and can be applied in cases other than the "biquad."

Yet another "biquad" technique is the so-called SAB or Single-Amplifier-Biquad which is fairly difficult to design, but which uses only one op-amp. Fig. 6-10 shows the general idea. Basically, this is an extension of the multiple-Feedback Infinite-Gain bandpass circuit, as was discussed in Chapter 5.

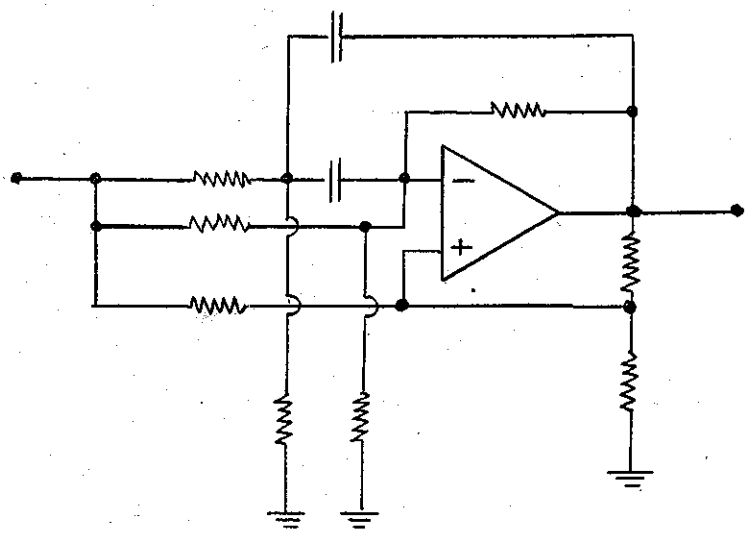


Fig. 6-10

Structure of the Single Amplifier Biquad

6-4 ACTIVE LADDER METHOD NO. 2 - SIGNAL-FLOW-GRAPH REALIZATION:

In Chapter 5, we looked at a method of using a passive ladder as a prototype for an active filter. The idea was to take advantage of the excellent passive sensitivity of these ladder networks, so that higher order filters (say 10th - 16th order) can be realized. In Chapter 5, we did this by simulating the inductors with gyrators, or by using the "supercapacitor" (FDNR) approach. Here we will be simulating the signal flow graph (SFG) of the network rather than the network itself. The method is in many ways similar to the state-variable approach.

The SFG of a network may well be a familiar concept to the reader, but it can also be learned from the material presented here. Fig. 6-11a shows the same passive network that was considered in Chapter 5. We will develop the signal flow graph of this network (Fig. 6-11c) and then realize it with op-amp integrators (Fig. 6-12b). The analysis of Fig. 6-11a begins by writing down the network analysis equations, which are listed in Fig. 6-11b. There are seven such equations, corresponding to the seven unknowns I_1, I_2, I_3, I_4, I_5, V_2, and V_3, and each is either an "Ohm's Law" relationship or a current summing relationship. Of course, the equations can be arranged into some different forms, but if we are only going to solve them, this is not too important. If we do solve the network analysis equations (by one of numerous procedures that work), we arrive at the transfer function:

$$T(s) = \frac{1/C_1C_2R_1L}{s^3 + s^2\,\frac{(C_1R_1 + C_2R_2)}{R_1R_2C_1C_2} + s\,\frac{[L + R_1R_2(C_1+C_2)]}{R_1R_2C_1C_2L} + \frac{R_1+R_2}{R_1R_2C_1C_2L}} \qquad (6\text{-}27)$$

which is a third-order low-pass which was also seen in Chapter 5.

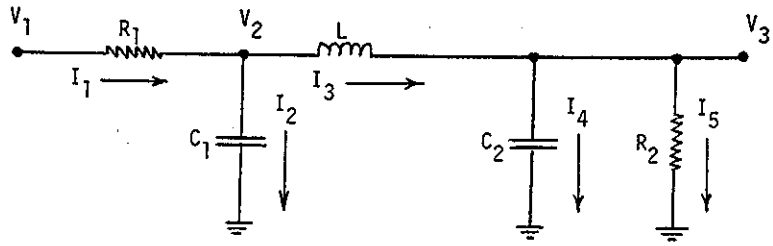


Fig. 6-11a
Original Passive Ladder

Network Analysis Equations

$I_1 = (V_1-V_2)/R_1$
$I_2 = V_2/(1/sC_1) = V_2sC_1$
$I_3 = (V_2-V_3)/sL$
$I_1 = I_2 + I_3$
$I_4 = V_3/(1/sC_2) = V_3sC_2$
$I_5 = V_3/R_2$
$I_3 = I_4 + I_5$

Rewritten for Flow Graph

$I_1 = (V_2-V_1)/R_1$
$V_2 = I_2/sC_1$
$I_3 = (V_2-V_3)/sL$
$I_2 = I_1 - I_3$
$V_3 = I_4/sC_2$
$I_5 = V_3/R_2$
$I_4 = I_3 - I_5$

Fig. 6-11b
Network Equations

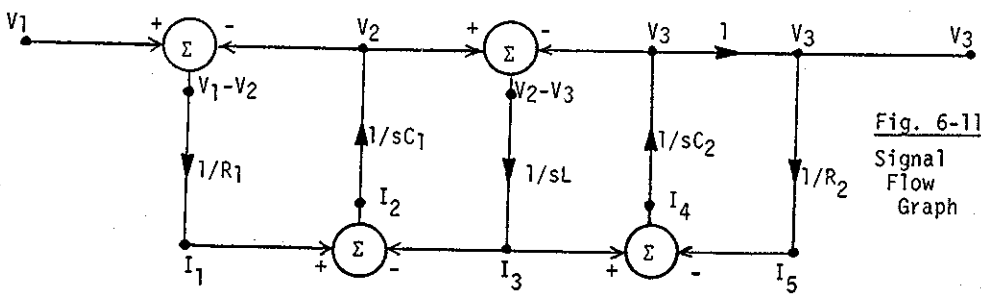


Fig. 6-11c
Signal Flow Graph

Here however we intend to work with the network equations and draw an equivalent SFG for the network. To do this, we have rewritten the network equations in Fig. 6-11b on the right side. The basic thing we are trying to do here is to write all equations that contain an s as integrators, since eventually we want to only have integrators. Secondarily, we expect that the input to the integrators (the numerators of the equations that have s in the denominator) will be summations. Accordingly the current summation equations are rearranged so that this is explicitely seen. We should not suppose that there is only one way to do these procedures. If we do something backward, we will likely see a problem when we try to draw the flow graph, and be able to reverse it then.

Fig. 6-11c shows the signal flow graph that corresponds to the equations of Fig. 6-11b. By going through the entire list, it can be seen that each and every one of the seven equations is represented. Note that the path multipliers (the arrowheads) correspond to multiplication by an impedance going up, and division by an impedance going down. Correspondingly, the voltage variables appear in the top portion of the graph, while current variables appear in the bottom portion. While it can be easily verified that the SFG is correct for the network, a couple of points can be made about how this SFG is actually obtained. The first point is that in general, you will get a neat and useful graph only after several preliminary sketches and redrawings (or by mimicking an example such as the one here). Secondly, other general forms are both possible and common. One such form places all the "state-variables" in a straight line, such as V_1, I_1, V_2, I_3, V_3, with the summers and multipliers in their proper positions in the line. In such a case, the paths going to the (-) inputs of the summers appear as backward loops of negative feedback, which is a useful point of view. Note however that the "topology" is identical for all these variations, and all realizations will at least be equivalent, differing in efficiency.

Having now obtained a correct flow graph, we need to find a realization of the flow graph. Note that the flow graph describes the relationship between the "state variables" (the voltages and currents) of the network. We can think of these state variables as just numbers, related by the flow graph. However, it is more to the point here to think of them all, voltages and currents alike, as being voltages. We can make the flow graph reflect this by multiplying all downward path multipliers by some resistance R, and all upward path multipliers by 1/R. This means that the lower portion of the flow graph is now also voltage, and no longer current. All path multipliers are now dimensionless, and the integration paths now have actual time constants showing. This change is seen in converting Fig. 6-11c to Fig. 6-12a. However, there are also other changes that have been made, and these will be discussed. The additional changes have been made so that Fig. 6-12a serves as a more natural link between the first flow graph (Fig. 6-11c), and the final realization (Fig. 6-12b).

In anticipation of the use of the simplest possible hardware structures (such as inverting integrators), we will want to make some sign changes. We can change a sign at any point we find it convenient, provided we make compensating changes elsewhere as needed. Hopefully the compensating changes may also improve things, or at least make them no worse. A full set of such changes have been employed in reaching Fig. 6-12a. Because these changes can be a matter of some confusion, a step-by-step diagram of these changes is shown in Fig. 6-13 as a matter of reference. The overall goal of the sign changes is to achieve as many inverting integrators as possible, and to have all summers entered with the same polarity. In Fig. 6-12a, we have been able to make two of the three integrators inverting, and all summer polarities are (+). [Note that the center integrator has an extra power of R, top and bottom, so as to show a time constant in the denominator. We will see how this works out later.]

Our final step is to convert our flow graph into an op-amp circuit, and we would like to do this as simply, and with as few components, as possible. Since all the flow graphs we have drawn are theoretically equivalent, we could jump to the realization from any one of them. However it is clear that we have been modifying with some purpose in mind, and this we have done by thinking of the eventual hardware to come. (Glancing at Fig. 6-12b, we see that we end up with just four op-amps).

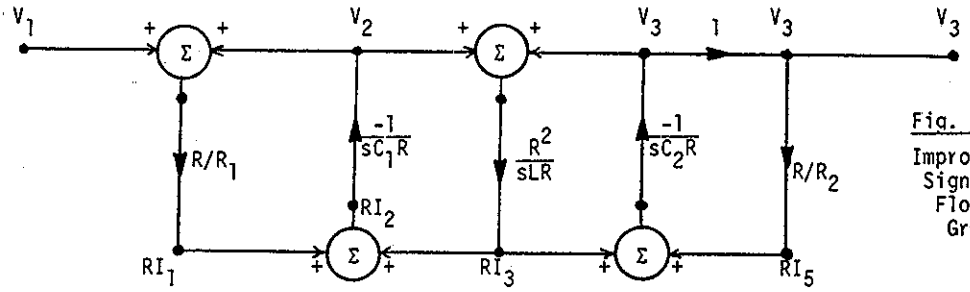


Fig. 6-12a
Improved Signal Flow Graph

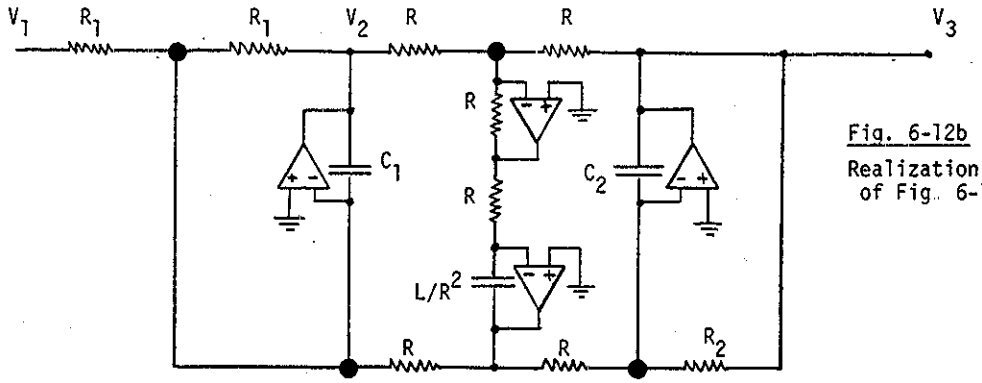


Fig. 6-12b
Realization of Fig. 6-12a

However, let's suppose that we had not done this simplification already, but instead started with the first realizable form, which would be Fig. 6-13a. This flow graph has four differential summers (involving one or two op-amps each), and three non-inverting integrators (with two op-amps each, or three extra capacitors overall). If we go about this blindly, as many as a dozen or more op-amps will be used. Obviously, this would be a bad place to stop with this approach. What might then happen would be that the designer, following good engineering practices, would look at the circuit that is believed to work, and ask if it is possible to simplify it. In so doing, many op-amp structures could be eliminated as redundant, and it is even possible that the circuit of Fig. 6-12b would be the final result.

Since we have gone to some effort to reach the best version of the flow-graph for our purposes, we can begin with Fig. 6-12a. Fig. 6-12b shows how this is converted to the op-amp realization. Here we are using current summing nodes ("virtual grounds") to do our summing - these nodes being indicated by the heavier dots in Fig. 6-12b that are positioned directly below the corresponding summers of Fig. 6-12a. Note that the two leftmost summers of Fig. 6-12a are actually one three input summer, and appear as two separate heavy dots in Fig. 6-12b, although it is only one summing node in reality. Here the summing nodes of the integrators themselves are being used, as it would be a waste to use separate summers. The center integrator uses an inverter, as this one must be non-inverting overall. The order of the two op-amps in the center branch is arbitrary however.

This probably covers all but two points. The first has to do with the way the non-unity ratios (R/R_1 and R/R_2) are realized as path multipliers. Clearly this is a change of gain, as seen in Fig. 6-12a, while it appears as a change of time-constant in Fig. 6-12b. We recall however the discussion of integrators where the equivalence between gain and time-constant was discussed. Accordingly, changing the integrator resistor from R to R_1, for example, changes the time constant from RC to R_1C, which is equivalent to changing the gain from 1 to R/R_1, which is what we wanted.

The final point relates to the strange-looking capacitor in Fig. 6-12b, which has the value L/R^2. What is implied here is that the numerical values are to be used. In our passive network, we assume that we know all the element values, and we would plug in the numbers to obtain a capacitor which we might call "C_3" for the center integrator. Incidentally, the units of L/R^2 are those of capacitance, so the conversion is completely valid.

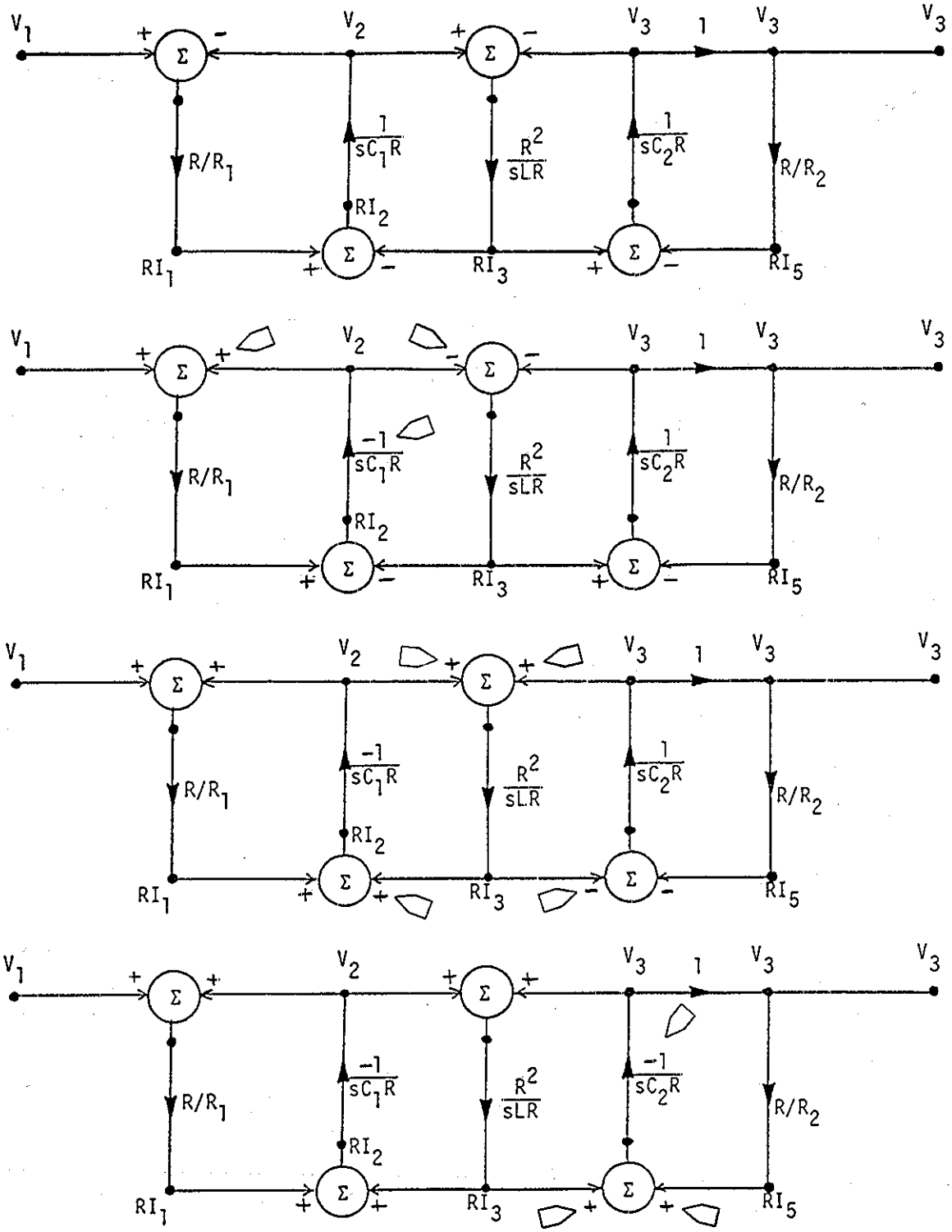


Fig. 6-13 Original signs (a) followed by adding inverting integrator (b) with two compensating changes. Middle integrator is left non-inverting, but two inputs and two outputs are all changed in sign (c). The two remaining (-) signs on the lower right summer can then be incorporated into the integrator that follows, making it inverting (d). Fig. 6-13d is same as Fig. 6-12a. ▷ indicates points where sign changes are being made.

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