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ELECTRONOTES MUS. ENG. GROUP
213 DRYDEN ROAD
ITHACA, NY 14850
(607) - 273-8030

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# MORE CLOCKING OSCILLATORS FOR DIGITAL IC'S

A number of digital clocking circuits were discussed in AN-27. One of these circuits is shown in Fig. 1. Since the switching point of the CMOS inputs is at approximately $V_S/2$, we can see how the RC charging circuit sets the frequency of oscillation.

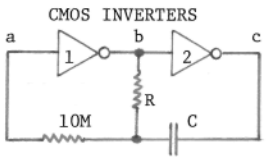
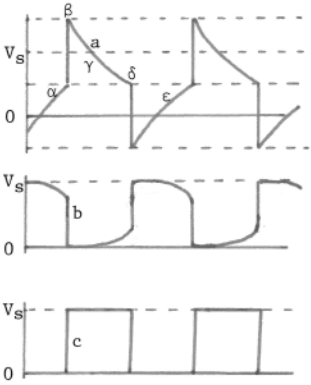



FIG. 1

The timing diagram of the various waveforms in the circuit are shown below the circuit in Fig. 1. Note that the waveform "c" is the most conventional looking digital signal. However, we will start by considering what is happening as the waveform at "a" approaches the $V_S/2$ point at α. As soon as it starts to cross the $V_S/2$ level, the output of inverter 1 will start going low, and this will in turn cause inverter 2 to go high. The capacitor C retains momentairily whatever voltage it had, and is elivated by this rise of inverter 2, and ends up at the point β, which is above the supply rail at $3V_S/2$. The capacitor then starts to discharge along the curve (γ) with its RC time constant, discharging toward the ground potential of waveform "b". Note that waveform "b" starts to round up as "a" approaches $V_S/2$. This is due to the fact that the CMOS input becomes more linear as its voltage approaches $V_S/2$. Note that "a" discharges from $3V_S/2$ to $V_S/2$, which is 2/3 of the way down, and requires a time of 1.1RC. When waveform "a" reaches δ, inverter 1 goes high, inverter 2 goes low, and this low transition couples through C and waveform "a" ends up at $-V_S/2$. After another time 1.1RC, we end up at ε, which is the same point as α, and the cycle is completed. The total time of the cycle is thus 2.2RC, and the frequency is:




$$F = \frac{1}{2.2RC}$$

The analysis of the circuit above serves to show how this type of circuit works, and also demonstrates several other points. Note that the waveform "a" exceeds the supply limits as a result of differentiation by the capacitor C. If the 10M resistor is replaced by a short, the circuit will still work, but the protection diodes on the CMOS input will clip this excess off at the supply voltages ($+V_S$ and ground) with the result that the RC discharge time is to only 1/2 rather than 2/3. This means that the frequency goes up, and is given by 1/1.38RC. However, the circuit of Fig. 1 is recommended because it does not rely on the protection diodes to operate properly. This works as predicted as long as $R << 10M$. A second thing to note is that the waveform "a" is hardly what you would call a digital waveform, "b" is better, and "c" is better still. In this type of circuit, the waveform tends to get more and more square the further you get from the R-C Junction. For this reason, it is often desirable to have additional gates or inverters in a loop for the oscillator, or to have them follow the ocsillator. This is particularly important if the outputs of the oscillator are to be used directly, or if a second phase of the oscillator is needed. For example, "b" and "c" above are out of phase, but we would not consider them otherwise equal because of the rounding of the "b" waveform.

Two oscillators with additional inverters in the loop are shown in Fig. 2 and Fig. 3. Note that Fig. 2 is just like Fig. 1, except the R and C are reversed, and an extra inverter has been added. Fig. 3 is exactly like Fig. 1 except two extra inverters have been put in series with inverter 1. In general, you can expect experimental measurments of frequencies to be a little below the theoretical ones, and in general, adding one or two extra inverters will improve this - that is, the frequency may go up by a percent or so even though there is more delay in the loop. However, the main advantage of the extra inverters is that you get digital signals that are more square, and they can be removed from points that are relatively isolated from any of the outputs that determine the timing.

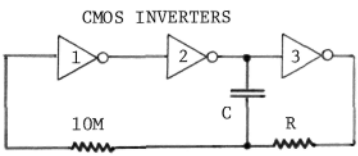


FIG. 2

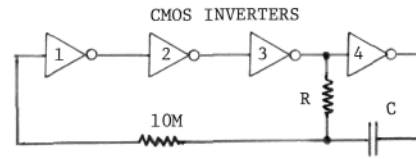


FIG. 3

It is probably clear from an examination of Fig. 1, Fig, 2, and Fig. 3 how the process can be extended to more and more inverters in the loop. If you are removing only one phase, use inverter 3 of Fig. 2, or inverter 4 of Fig. 3. For removing two phases, Fig. 3 is suggested, using the outputs of inverters 3 and 4. If it is essential that the timing circuitry be undisturbed, use the six inverter version of Fig. 3, removing the two phases from inverters 3 and 4 (inverter 5 drives R and inverter 6 drives C in the six inverter loop).

We have shown above only CMOS inverters in the oscillators. This is because things are very simple with CMOS, but not so simple with TTL. Of course, the same general form for the circuit still works with TTL, but you have to realize that the TTL inputs are very different from CMOS inputs. For one thing, you will have to use a short circuit in place of the 10M resistors. Of course, you can only work with a 5 volt supply. Also, in general, R can only be 1k or less. Finally, the output waveform in general will not be close to a square wave (as it is with CMOS) and the frequency formula given above will only be very rough. However, if you don't mind playing around, you can get something close to what you need. Fig. 4 shows a TTL oscillator which runs about 40 KHz. A similar circuit using a 7405 (open collector TTL) is suggested by Don Lancaster in his TTL Cookbook and is sketched in Fig. 5. This oscillator is intended for use in the 1 to 10 MHz range.

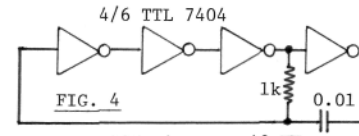


FIG. 4

TTL OSC. Approx. 40 KHz

Because of the superiority of CMOS, it is suggested that CMOS oscillators be used to drive TTL, or that the 555 be used. The 555 timer will drive TTL directly. While a single CMOS inverter, or a CMOS NAND gate will not drive TTL, two inverters or NAND gates in parallel, or a CMOS NOR gate will generally drive one TTL load to get things going. This opens up a lot of possibilities. A hex inverter can be used in Fig. 3 and the extra inverters can buffer to the TTL, or the circuit of Fig. 3 can be realized using a quad NOR gate as the CMOS inverters. While these are the general rules, there are cases where a single inverter may drive a TTL input - but you may only be lucky and it will stop later, or it may not work in the next circuit you try. Play it safe.

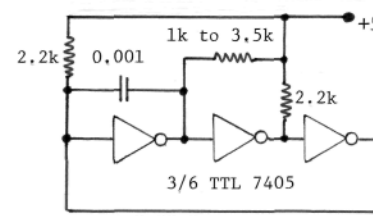


FIG. 5